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Reliability-Oriented Redundancy Design for Modular Multilevel Cascaded Converter-based STATCOMs

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À minha família, mentores e amigos.

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"Quando tudo está perdido,
Sempre existe uma luz."
Renato Russo

Resumo

Os sistemas de distribuição e transmissão de média/alta tensão possuem uma enorme variedade de cargas não lineares. Além disso, a grande penetração de fontes de energia renováveis no sistema elétrico tem motivado estudos relacionados ao compensador síncrono estático (STATCOM, do inglês *static synchronous compensator*). Nesse contexto, o conversor multinível é uma tecnologia interessante para esta aplicação. Uma atenção especial é dada aos conversores modulares multiníveis em cascata (MMCCs, do inglês *modular multilevel cascaded converters*) devido à alta escalabilidade, modularidade, redundância e eficiência, que são características inerentes à topologia. Para ser capaz de atuar em altos níveis de tensão, é necessário associar um grande número de células/dispositivos semicondutores, que pode afetar a confiabilidade do conversor. Células redundantes podem ser empregadas para atender aos requisitos de confiabilidade do conversor. No entanto, o projeto do fator de redundância ainda é um campo a ser explorado. Este trabalho propõe um modelo de confiabilidade para a seleção correta do número de células redundantes, visando atingir uma meta de vida útil determinada. Este modelo combina as análises de falhas aleatórias e falhas por desgaste. O fator de redundância é calculado para determinados requisitos de confiabilidade, ou seja, este trabalho propõe um projeto de redundância orientada a confiabilidade. O estudo de caso é baseado em um MMCC STATCOM de 13,8 kV/17 MVA. A implementação do conversor é baseada em quatro tensões de bloqueio comerciais de dispositivos semicondutores (1,7, 3,3, 4,5 e 6,5 kV). Os custos de capital (CAPEX, do inglês *capital expenditure*) e os custos operacionais (OPEX, do inglês *operational expenditure*) são estimados considerando o fator de redundância necessário. Considerando como objetivo 20 anos de operação para o conversor e níveis de confiabilidade maiores que 90%, o projeto baseado em dispositivos de 1,7 kV apresenta o menor custo para a realização do MMCC STATCOM.

Palavras-chaves: Conversor modular multinível em cascata; STATCOM; Confiabilidade; Redundância; Falhas por desgaste; Falhas aleatórias.

Abstract

Medium/high-voltage distribution and transmission systems have a huge variety of nonlinear loads. Additionally, the large penetration of renewable energy sources in the power system has motivated studies about static synchronous compensator (STATCOM). In this context, the multilevel converter is an interesting technology for this application. Particular attention is given to modular multilevel cascaded converters (MMCCs) due to the high scalability, modularity, redundancy and efficiency that are inherent features of the topology. To be able to operate at high voltage levels, a large number of semiconductor cells/devices is required, compromising the converter reliability. Redundant cells can be employed to fulfill the converter reliability requirements. However, the redundancy factor design is still an important area to be explored. This work proposes a reliability model for the correct selection of the redundant cells number, which aims to reach a determined lifetime target. This model combines random failure and wear-out failure analysis. The redundancy factor is computed for given reliability requirements, i.e., this work proposes a reliability-oriented redundancy design. The case study is based on a 13.8 kV/17 MVA MMCC-based STATCOM. The implementation of the converter is performed through four commercial blocking voltage of semiconductor devices (1.7, 3.3, 4.5 and 6.5 kV). The capital expenditure (CAPEX) and operation expenditure (OPEX) are estimated considering the required redundancy factor. Considering a target of 20 years of operation for the converter and reliability levels greater than 90%, the design based on 1.7 kV devices has the lowest cost for the MMCC STATCOM realization.

Keywords: Modular multilevel cascade converter; STATCOM; Reliability; Redundancy; Wear-out failures, Random failures.

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List of abbreviations and acronyms

ABB	Asea Brown Boveri (Swedish-Swiss multinational corporation)
ac	Alternating Current
ANPC	Active Neutral Point Clamped
CAPEX	Capital Expenditure
CDF	Cumulative Density Function
CHB	Cascaded H-bridge
COBEP	Brazilian Power Electronics Conference (Conferência Brasileira de Eletrônica de Potência)
dc	Direct current
DCMC	Diode Clamped Multilevel Converter
DFR	Design for Reliability
DSBC	Double-Star Bridge Cell
DSCC	Double-Star Chopper Cell
EMI	Electromagnetic interference
FACTS	Flexible ac transmission systems
FC	Flying Capacitor
FCMC	Flying Capacitor Multilevel Converter
FIT	Failure in time
GaN	Gallium Nitride
GE	General Electric
GESEP	Power Electronics and Power Systems UFV laboratory (Gerência de Especialistas em Sistemas Elétricos de Potência)
GTO	Gate Turn-Off Thyristors
HVDC	High-Voltage Direct Current

IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristors
LC	Life Consumption
MAF	Moving Average Filter
MMC	Modular Multilevel Converter
MMCC	Modular Multilevel Cascade Converter
MV	Medium Voltage
NPC	Neutral Point Clamped
OPEX	Operational Expenditure
PCC	Point of Common Coupling
PDF	Probability Density Function
PLECS	Piecewise Linear Electrical Circuit Simulation
PR	Proportional Resonant
PSC-PWM	Phase-Shifted Carrier Pulse Width Modulation
pu	Per unit
PV	Photovoltaic
PWM	Pulse-Width Modulation
RAC	Redundancy based on Additional Cells
RACO	Optimized Redundancy based on Additional Cells
rms	Root Mean Square
RSC	Redundancy based on Spare Cells
SC	Synchronous Condensers
SDBC	Single-Delta Bridge Cell
SiC	Silicon Carbide
Si-IGBT	Silicon Insulated Gate Bipolar Transistor

SiC-JFET	Silicon Carbide Junction Field-Effect Transistors
SR	Standard Redundancy operation
SSBC	Single-Star Bridge Cell
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TCSC	Thyristor controlled Series Capacitor
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

List of symbols

A_h	Heatsink surface area
$B_y(x)$	Operation time at which y percent of devices fail
C	Cell capacitance
C_{h-f}	Heatsink-to-fluid thermal capacitance
C_{17},C_{33},C_{45},C_{65}	Case studies for DSCC-MMCC based STATCOM
c_h	Specific heat capacity
D_1	Top anti-parallel diode of the chopper cell
D_2	Bottom anti-parallel diode of the chopper cell
d_h	Heatsink thickness
E_c	Converter energy consumption
$F(x)$	Unreliability function
f_c	Cell carrier frequency
f_{ef}	Effective converter output frequency
f_{fc}	Fluid flow convection coefficient
f_{ma}	Moving average filter frequency
f_n	Grid frequency
f_{us}	Device utilization factor
$f(x)$	Probability distribution function
$\widehat{I}_n$	Converter rated peak current
I_{svc}	Rated device current
i_{avg}	Average current of the converter arm
i_c	Converter circulating current
i_c^*	Converter circulating current reference

i_g	Grid current
i_l	Lower arm current
i_u	Upper arm current
$i_{u,rms}$	Uper arm current rms value
K_c	Price per switching power
K_o	Price per kilowatt-hour
k	Non-redundant cellsper arm
k_b	Proportional gain for individual balancing control
L_{arm}	Arm inductance
L_g	Equivalent grid inductance
m	Redundant cells per arm
m_i	Modulation index
$m_{i,max}$	Maximum modulation index
m_u	Ideal modulation signal of upper arm
$N(x)$	Number of surviving devices at time x
n	Number of cells per arm
P	Instantaneous active power
P^*	Instantaneous active power reference
Q	Instantaneous reactive power
Q^*	Instantaneous reactive power reference
R_{arm}	Arm resistance
R_b	Bleeder resistor
R_g	Equivalent grid resistance
R_{h-f}	Heatsink-to-fluid thermal resistance
$R_{cf}(x)$	Constant failure reliability function
$R_{kf}(x)$	Reliability function for *k-out-of-n* systems

$R_{wf}(x)$	Wear-out reliability function
$R(x)$	Reliability function
RF	Redundancy factor
S_n	Converter nominal power
S_T	Permanent bypass switch
S_1	Top IGBT of the chopper cell
S_2	Bottom IGBT of the chopper cell
T_a	Ambient temperature
T_c	Case temperature
T_j	Junction temperature
$T_{[j,c]m}$	Junction and case average temperature
t_{on}	Heating time
T_1	Step-up transformer
$\hat{V}$	Peak value of phase voltage
V_g	Line-to-line converter output voltage rms value
V_s	Line-to-line converter output voltage rms value
V_{sf}	Voltage stress factor
V_{svc}	Semiconductor blocking voltage capability
v_{avg}	Average voltage of all cell capacitors
v^*_{avg}	Reference value for average capacitor voltages
v_b	individual balancing voltage
v_c	Converter internal voltage
$v_{cell,i}$	Cell capacitor voltage
v_{dc}	Nominal converter dc-link voltage
v_g	Grid effective line-to-neutral voltage
$v_{g,\alpha\beta}$	Grid voltage in stationary reference frame

$v_{s,\alpha\beta}$	Equivalent output converter voltage in stationary reference frame
v_l	Lower arm voltage
v_s	Effective line-to-neutral voltage synthesized by the converter
v_u	Upper arm voltage
W_{conv}	Energy storage requirement
x	Operation time
x_0	Target operation time
Z_{c-h}	Case-to-heatsink thermal impedance
Z_{h-f}	Heatsink-to-fluid thermal impedance
Z_{j-c}	Junction-to-case thermal impedance
α	Maximum current rise rate
β	Shape parameter of Weibull distribution
β_c	Angular displacement between the carrier waveforms in the upper and lower arms
η	Scale parameter of Weibull distribution
Δi_c	Peak-to-peak circulating current ripple
$\Delta T_{j,c}$	Junction and case variation of temperature
κ_h	Thermal conductivity of the heatsink material
λ_b	Component base failure rate
λ_{IGBT}	IGBT module failure rate
$\lambda(x)$	Failure rate
μ	Mean value of normal distribution
π_A	Application factor
π_E	Environmental factor
π_S	Electric stress factor
π_T	Temperature factor

ϕ	Phase difference between grid voltage and current
ρ_h	Material density of the heatsink
σ	Standard deviation of normal distribution
$\theta_{l,n}$	Angular displacements of the lower carrier waveforms
$\theta_{u,n}$	Angular displacements of the upper carrier waveforms
θ_z	Angle that define the zero crossing of the current arm
ω_n	Angular grid frequency

Superscripts

$*$	Reference value
$'$	Equivalent static value

Subscripts

u	Upper arm
l	Lower arm

Contents

1 Introduction

1.1 Context and Relevance

The distribution and transmission systems are complex structures that require careful operation, design and planning. Nowadays, the connection of various nonlinear loads (such as electric arc furnaces, electric locomotives, variable frequency speed of controlling high voltage large motor, high-power full controlled devices, etc.) makes the grid voltage fluctuate frequently and results in power quality deterioration (Ma; Huang; Zhou, 2015). In addition, the massive penetration of renewable power plants (solar, wind, etc) affects the power quality, increasing the fluctuations in point of common coupling (PCC) (Blaabjerg et al., 2006). Furthermore, the increase in power demand and interconnected transmission systems implies strict requirements of reliability, operation and control.

Reactive power (Var) compensation is indicated to improve the performance of ac power systems at the transmission and distribution levels (Benidris et al., 2016). The reactive power compensator is usually controlled in two different modes: Load compensation mode and voltage support mode (Ma; Huang; Zhou, 2015). The load compensation aims to increase the value of the system power factor, eliminate harmonic current components produced by large and fluctuating nonlinear industrial loads (Dixon et al., 2005). On the other hand, voltage support is generally required to reduce voltage fluctuation at a given terminal of a distribution or transmission line.

Flexible ac transmission systems (FACTS) have been developed to improve the performance of weak ac systems and to enhance transmission capabilities over long ac lines (Shahgholian et al., 2010). Generally, two types of compensation can be used: series and shunt compensation. Series compensation modifies the transmission or distribution system parameters, while shunt compensation changes the equivalent impedance of the load (Dixon et al., 2005). In both cases, the performance of the overall ac power system can be improved by controlling the reactive power exchanged with the power system.

Figure 1 (a) presents the diagram for series compensation. Thyristor controlled series capacitor (TCSC) and static synchronous series compensator (SSSC) are examples of devices used for series compensation. Figure 1 (b) illustrates the diagram for shunt compensation. Due to simplicity and low cost, switched capacitor/inductor banks are widely used as shunt compensators. However, these topologies are not fully controlled, limiting their use to situations where the reactive power compensation range is low (Dixon et al., 2005). The Static Var Compensator (SVC) can compensate lead and lag reactive power variably by controlling the thyristor switching angle aiming to solve this issue.

Nevertheless, the SVC generates low order harmonic currents to the grid by the thyristor firing, which requires a large amount of passive filters (Igbinovia et al., 2015).

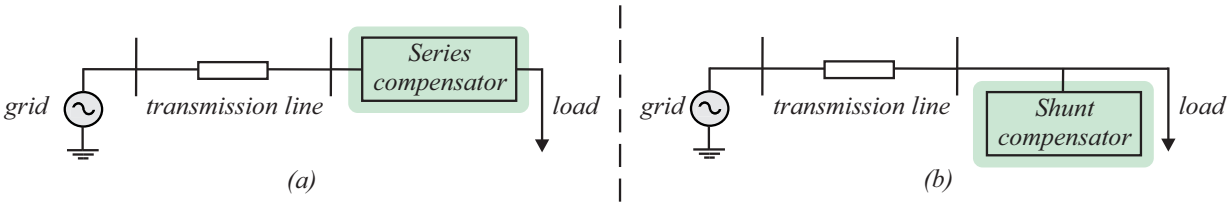

Figure 1 – Schematic of FACTS controllers for reactive power compensation: (a) series compensation; (b) shunt compensation.

Another shunt compensation technology is the Synchronous Condenser (SC). A synchronous machine connected to the power system which can exchange reactive power. However synchronous condensers require substantial foundations and a significant amount of starting and protective equipment (Igbinovia et al., 2015). Besides, they contribute to the short-circuit current, have slow response in case of rapid load changes, higher losses and operating expense than other technologies of reactive power compensation.

The Static Synchronous Compensator (STATCOM) is one of the most promising technology recommended for reactive power compensation in electrical power networks (Igbinovia et al., 2015; Ma; Huang; Zhou, 2015; Shahnia; Rajakaruna; Ghosh, 2014). This technology consists of a Voltage Source Converter (VSC) which exchanges reactive power with the grid. In comparison to SVC, STATCOM presents higher power density, higher efficiency and no contribution to short-circuit currents (Chakraborty et al., 2012). In addition, a fast dynamic response is achieved because mechanical inertia as in traditional synchronous compensators is avoided. These features make the STATCOM an interesting candidate for reactive support during fast transients.

The main drawback of STATCOMs is the higher cost, when compared to SVC systems. Nevertheless, the technical benefits and recent advances in power converters technology lead to the use of VSC topologies instead of thyristor based systems (Behrouzian, 2016). Table 1 summarizes the main features observed in the FACTS controllers (Kadandani; Maiwada, 2015).

1.2 STATCOM Realization

The major challenge in STATCOM realization is to design a converter topology which must reach high power and voltage levels with standard rated semiconductor switches (Fujii; Schwarzer; De Doncker, 2005; Muñoz et al., 2014). This section describes the development of STATCOM application based on two-level converters up to multilevel converters.

Table 1 – Comparison among FACTS controllers.

Device	Dynamic of response	Power quality	Steps	Inertia	Cost
Switched capacitors/ reactors	Slow	Low	Fixed	No	Low
Thyristor switched capacitors	Fast	Low	Fixed	No	Medium
Thyristor controlled reactor	Fast	Low	Continuous	No	Medium
SVC	Fast	Low	Continuous	No	Cheaper than STATCOM
Synchronous condenser	Fast	High	Continuous	Yes	High
STATCOM	Fast	High	Continuous	Possible	High

1.2.1 Two-level Converters

Initially, STATCOMs were implemented by two-level voltage source converters, as illustrated in Fig. 2 (a). A step-up transformer (T_1) is usually connected to the STATCOM output to allow the connection to medium voltage (MV) (Shahnia; Rajakaruna; Ghosh, 2014). However, these converters require relatively high switching frequency to deal with the harmonic distortion requirement, which results in high power losses. Moreover, a significant stress is caused in the ac terminal due to high voltage slope, as observed in Fig. 2 (b). In addition, when the voltage level increases to some kilovolts, this topology is less useful, due to the semiconductor blocking voltage range commercially available. Despite advances in silicon carbide (SiC) and gallium nitride (GaN) devices, the application field of this topology is still limited (Fujii; Schwarzer; De Doncker, 2005). Typical high-power silicon IGBT modules with 6.5 kV maximum blocking voltage are commercially available. This rating is not enough for two-level converters, which are connected directly to the grid of more than a few kV units.

One solution is the series connection of power devices to increase the blocking voltage capability, as illustrated in Fig. 3 (a). Nevertheless, this solution is very complex due to some practical issues, such as voltage equalization between the series switches and fault-tolerant operation (Shammas; Withanage; Chamund, 2006). To perform voltage equalization, snubber structures are usually required, which increase the converter switching losses (Shahnia; Rajakaruna; Ghosh, 2014). Since press-pack devices guaranteed short-circuit failure mode, they can be employed to increase the fault tolerance capacity (Ladoux; Serbia; Carroll, 2015). However, this technology is not commercialized by many manufacturers, which lead to high cost for the series connection solution.

The use of multi-stage transformer topology is another solution. As observed in Fig. 3 (b), several two-level converters are connected to the transformer (Fujii; Schwarzer; De

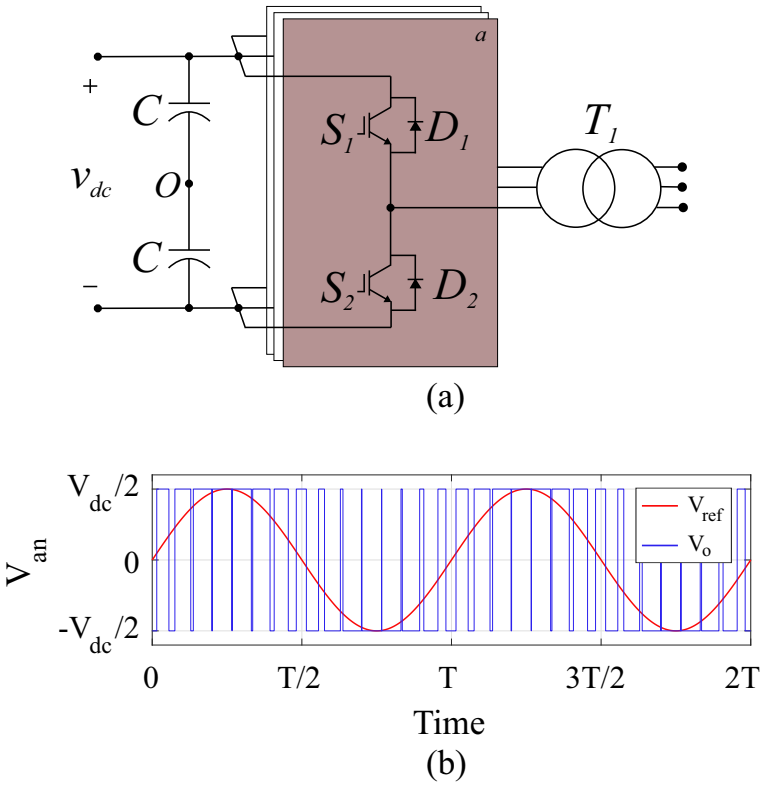

Figure 2 – Two-level voltage source converter: (a) Schematic of the three-phase circuit; (b) Two-level output voltage.

Doncker, 2005). However, this transformer makes the STATCOM bulky and heavy, and affects the overall efficiency (Hagiwara; Akagi, 2009). According to Fang Zheng Peng et al. (1995), field experiences show the transformer can produce about 50% of the total losses, occupy up to 40% of the system space and hamper the control due to inrush currents and saturation effects.

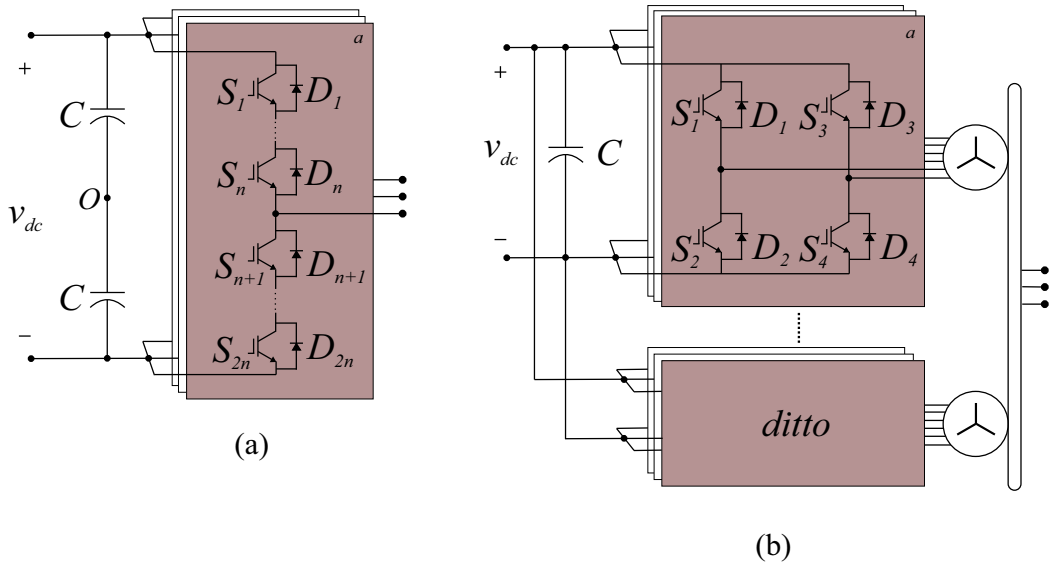

Figure 3 – Two-level voltage source converter: (a) with series connection of semiconductor switches; (b) with a Multi-Stage Transformer.

1.2.2 Early Multilevel Converters

In conventional use of STATCOM, the converter voltage is increased through a step-up transformer before connecting to grid. Consequently the current will be high in the low voltage side which leads to higher power losses. This fact led the research community to focus on transform-less solutions, to directly connect the converter into the grid (Behrouzian; Bongiorno; Zelaya De La Parra, 2013). A widely used alternative for medium/high-voltage systems is the multilevel converters. The multilevel converter employs medium-voltage devices to obtain a converter with higher voltage capability. The following advantages of multilevel topologies can be highlighted (Franquelo et al., 2008):

- Low switching frequency can be employed, which results in high efficiency;
- A high number of levels can be reached, resulting in low harmonic contents in the output voltage and current;
- Low voltage steps (dv/dt), which reduce stresses in the insulation of any equipment connected at the converter output;
- High power density, since the output filters can be reduced or even removed in some cases.

There are a limited number of topologies that provide multilevel voltages and are suitable for medium voltage applications. The topologies with considerable commercial success are the neutral point clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB) (Fujii; Schwarzer; De Doncker, 2005). Other topologies such as the hybrid converters have been proposed as well, but they are not fully accepted for industrial applications (Barbosa et al., 2005).

The neutral point clamped (NPC) converter, or diode clamped multilevel converter (DCMC) in three-level version, was the first multilevel converter employed in large scale (see Fig. 4) (Nabae; Takahashi; Akagi, 1981). However, when more than three voltage levels are necessary, some clamp diodes must block more than two times the IGBT voltage, the number of interconnections between the converter switches also increases and the mechanical design of the converter becomes more complex (Fujii; Schwarzer; De Doncker, 2005; Sharifabadi et al., 2016). In addition, the inherent imbalance in the series connected dc capacitors requires an external balancing circuit (Hagiwara; Akagi, 2009). Therefore, the number of levels is usually limited to five or seven levels in practical applications (Fujii; Schwarzer; De Doncker, 2005). Other inherent problem in the NPC topology is the thermal unbalance between the outer and inner devices of each phase. The active neutral point clamped (ANPC) converter was introduced to solve this particular issue (Bruckner; Bemet, 2001). In this topology, the clamping diodes (D_5 and D_6) are replaced by active

switches. Under such conditions, the zero voltage state can be implemented with more possibilities, which results in a thermal balance between the converter switches (Bruckner; Bemet, 2001).

The flying capacitor multilevel converter (FCMC) was introduced by (Meynard; Foch, 1992). This converter requires a pre-charge on the capacitors at startup. Also, for higher number of levels, the voltages at the flying capacitors differ. These features make practical applications limited to low levels in medium voltage systems (Sharifabadi et al., 2016).

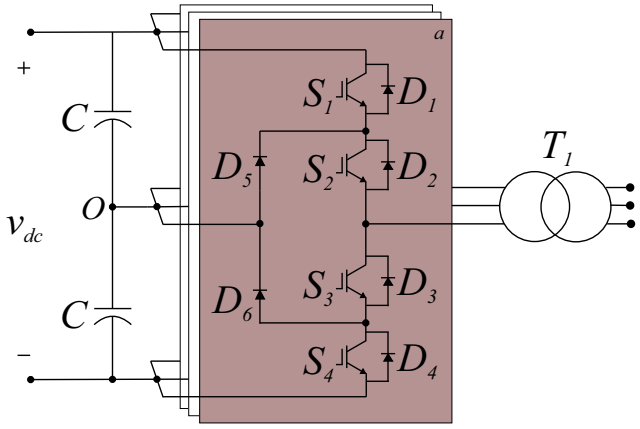

Figure 4 – Three-phase three-level NPC converter with step-up transformer.

1.2.3 Cascaded Multilevel Converters

To overcome the limitations found in other multilevel topologies, cascaded multilevel converters (Mcmurray, 1971; Marquardt, 2001; Lesnicar; Marquardt, 2003) are an attractive solution to provide a voltage source converter for STATCOM realization. This topology is based on cascaded connection of cells (also called submodules) to build up the output voltage. Figure 5 shows the single-line diagram of a cascaded H-bridge (CHB) converter. These converters also feature a high modularity degree because each cell can be seen as a module with similar circuit topology, control structure, and modulation. Therefore, in the case of a fault in one cell, replacement and maintenance is quick and easy (Behrouzian; Bongiorno; Zelaya De La Parra, 2013). Moreover, the faulty module can be bypassed without interrupting the operation, bringing an almost continuous overall availability and high reliability. Behrouzian, Bongiorno and Zelaya De La Parra (2013) present the main features observed in the most suitable VSC topologies for STATCOM applications, as observed in Tab. 2.

Cascaded connection of bridge cells date back to the 1970s for single-phase systems (Mcmurray, 1971; Baker; Bannister, 1975). A three-phase STATCOM based on star-connected cascaded multilevel converter was proposed in 1996 by Fang Zheng Peng et al. (1995). For high power STATCOMs, Alstom marketed the converter based on gate

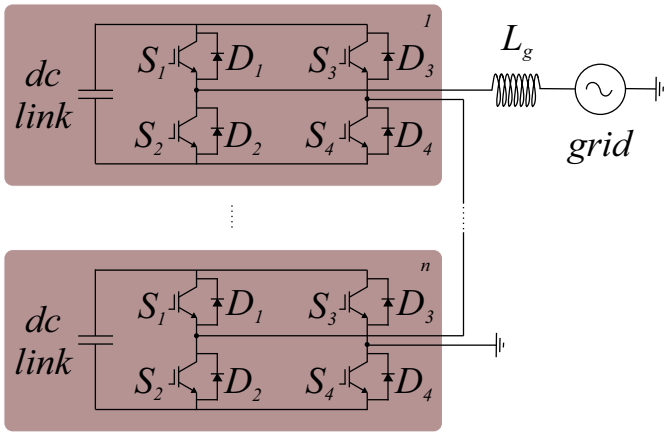

Figure 5 – Single-line diagram of (2n+1) level CHB.

Table 2 – Most suitable VSC topologies for STATCOM applications.

Topology	NPC	FC	CHB
Common dc link	Yes	Yes	No
Number of levels	3-5 levels	5-7 levels	No theoretical limit
Efficiency	Medium	Medium	High
Reliability	Low	Low	High
Modularity	No	No	Yes
Loss distribution	Unequal	Uniform	Uniform

turn-off (GTO) thyristors employed in the full bridges (Ainsworth et al., 1998). Nowadays, this concept is widespread in the industry and most products are based on IGBTs (Insulated Gate Bipolar Transistors) or press-pack IGCTs (Integrated Gate-Commutated Thyristors) (Sharifabadi et al., 2016).

The modular multilevel converter (MMC) is the most recent technology which was first introduced in 2001 (Marquardt, 2001). The MMC presents a dc-link, as observed in traditional two-level converters, while maintaining the important benefits of cascaded multilevel converters (Lesnicar; Marquardt, 2003). Akagi (2011) presented a classification and terminology of what is referred to as Modular Multilevel Cascade Converter (MMCC) family, which includes MMC and CHB converters in the same family. The MMCC family is classified into four topologies:

- Single-star bridge cell (SSBC), presented in Fig. 6 (a) with the cell of Fig. 6 (d);
- Single-delta bridge cell (SDBC), presented in Fig. 6 (b) with the cell of Fig. 6 (d);
- Double-star bridge cell (DSBC), presented in Fig. 6 (c) with the cell of Fig. 6 (d);
- Double-star chopper cell (DSCC), presented in Fig. 6 (c) with the cell of Fig. 6 (e).

Table 3 presents some STATCOMs currently available in the market. As observed, the major companies in the sector of STATCOMs provide some solutions based on cascaded

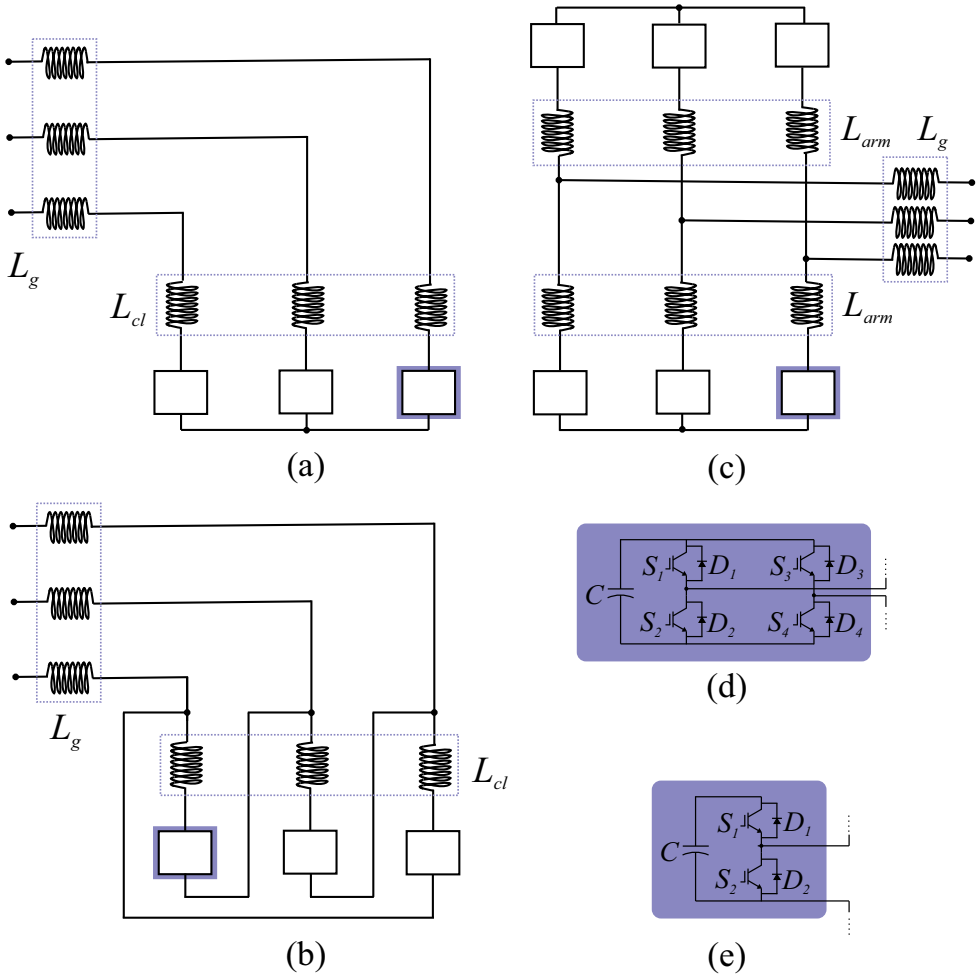

Figure 6 – MMCC configuration. (a) SSBC; (b) SDBC; (c) DSCC or DSBC; (d) Bridge Cell; (e) Chopper Cell.

multilevel converters. Indeed, STATCOMs are always in hot stand-by and the operational costs due to energy losses are very important. Therefore, cascaded multilevel converter topologies are widespread in the industry due to the high efficiency.

Table 3 – VSC topologies for STATCOM applications.

Converter Configuration	**Trade Mark**	**Manufacturer**
Two-level VSC + Transformer	VArPro^{TM}	ABB
	PCS 100	ABB
	SVG Statcom	Severn
Three-level VSC (NPC) + Transformer	PCS 6000	ABB
	MaxSine	GE
	GRIDCON®	MR
SDBC-MMCC	SVC Light	ABB
	GE-STATCOM	GE
	SVC Plus	Siemens
	SMART Q^{TM}	Hyosung

1.3 Trends for STATCOMs

The latest research efforts have focused on cascaded multilevel converters based STATCOMs for medium and high voltage systems. Currently, research on STATCOM is motivated by some factors such as cost reduction, system reliability and modern grid codes requirements.

1.3.1 Cost Reduction

First, cost reduction is very important for STATCOMs. Converter cost is directly related to the capital expenditure (CAPEX) and operational expenditure (OPEX). The CAPEX is related to investment in power electronics (e.g., semiconductor devices, controls, cabinets) (Siddique et al., 2016). Moreover, OPEX is associated with the devices power losses, maintenance and faulty device replacement (Tu; Yang; Wang, 2019). These factors drive research that seek to increase the converter reliability (Hui et al., 2019; Tu; Yang; Wang, 2019; Zheng et al., 2019) and STATCOM efficiency (Koyama et al., 2018; Hahn et al., 2018; Farias et al., 2018; Cupertino et al., 2019).

Saif et al. (2018) shows that most of the converter CAPEX is related to semiconductor devices when few levels are employed for medium voltage three-phase SSBC based STATCOM. Moreover, a larger number of levels in the converter can be employed aiming to reduce the semiconductor costs (Saif et al., 2018). However, combining a large number of semiconductor devices can compromise the converter reliability (Tu; Yang; Wang, 2019; Farias et al., 2019). Thus, there is a compromise relationship to consider when more cells are required and the most suitable reliability-cost trade-off should be chosen.

1.3.2 Reliability Requirements

The questionnaire survey is an effective way to collect reliability information from power electronic industries (Yang et al., 2011; Falck et al., 2018). Yang et al. (2011) conducted a survey with semiconductor manufacturers, integrators, and users in the aerospace, automation, motor drive, utility power, and other industry sectors to address concerns related to the requirements and expectations of reliability in power electronics. As observed, Figure 7 shows that “semiconductor power devices” was selected by 31% of the responders as the most fragile component. In addition, many industry survey participants were asked to define the elements that are most crucial to be researched to improve the reliability of power electronics converter systems (Falck et al., 2018). 40% of participants wished to see more research focused on power semiconductors and power semiconductor modules.

Regarding OPEX, many works present solutions to increase the efficiency of converters for STATCOM application (Hahn et al., 2018; Koyama et al., 2018; Farias et

al., 2018). In Hahn et al. (2018), different modulation methods with various capacitor designs are investigated for a DSCC-MMCC-based STATCOM application. As result, an individual trade-off has to be done between the cell capacitance (investment costs) and the cell switching frequency (operation costs). Koyama et al. (2018) present a comparison between cascaded multilevel converter configuration with Si-IGBT, SiC-JFET and hybrid configuration. Comparisons revealed that the hybrid configuration performs well in terms of loss and volume. Farias et al. (2018) present a power losses comparison for different redundancy strategies of DSCC-MMCC.

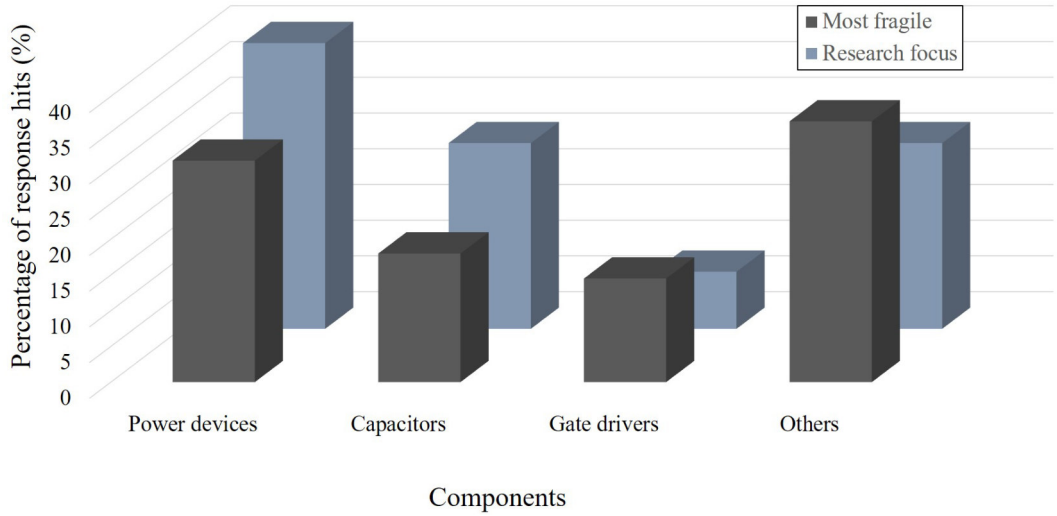

Figure 7 – Industry experts' answers to the: Black - distribution of fragile components in power converters; Blue - the components of power electronic systems that should focus on future research. Adapted from Yang et al. (2011), Falck et al. (2018).

1.3.3 Modern Grid Codes Requirements

The third factor is related to the modern grid codes for renewable energy power plants that require negative sequence support during voltage sags (VDE, 2015). In Germany, for example, the technical requirements for connection in the high voltage system imposes positive and negative sequence injection during unbalanced faults, as observed in Fig. 8. Therefore, the STATCOM converter must provide some negative sequence injection (Wijnhoven et al., 2014). According to Behrouzian and Bongiorno (2017), SSBC-MMCC and SDBC-MMCC present a singular operation point during unbalanced conditions. If the system reaches this point, the converter will probably trip from the electrical grid and will not be able to provide voltage support (Behrouzian, 2016). Moreover, (Cupertino et al., 2019) shows that when negative sequence components were compensated by STATCOM, the DSCC-MMCC topology presents low power losses compared to SDBC-MMCC. Under such conditions, double star topologies can be employed to deal with this issue.

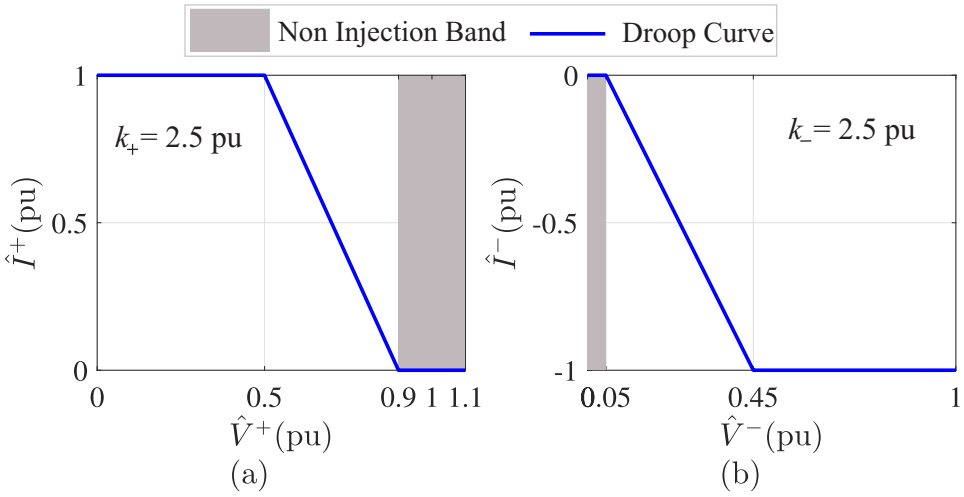

Figure 8 – Low voltage ride through current injection in Germany: (a) Positive sequence injection requirements; (b) Negative sequence injection requirements. Adapted from VDE (2015).

1.4 Purpose and Contributions

One advantage of MMCC-based topologies is the inherent fault-tolerant operation associated with the high number of cells. To ensure that the converter remains operational at this condition, a redundancy strategy needs to be included to the converter structure (Tu; Yang; Wang, 2019). Nevertheless, the redundancy factor selection to support a converter fault tolerance operation is an important field to be explored. Therefore, the main objective of this master thesis is to present a converter reliability-oriented model based on redundancy strategy aiming to improve cost reduction and reliability of MMCC-based STATCOMs. The following topics will be approached in this work:

1. *Modeling, Control and Design for DSCC-MMCC-based STATCOMs*: this topic proposes a design of DSCC-MMCC-based STATCOM. Analysis of number of cells, required cell capacitances, required current ratings of semiconductors power devices and output filter design are developed. Moreover, a dynamic response analysis of the converter is presented.

2. *Combined Reliability Design of DSCC-MMCC-based STATCOMs*: this topic proposes to combine the failure probabilities of semiconductor power devices, to evaluate the DSCC-MMCC system-level reliability. Regarding semiconductor devices, a reliability model that combines both wear-out and random failures data is applied.

3. *Reliability Evaluation Based on Redundancy Strategy*: the redundancy factor selection to support a converter fault tolerance operation is an important field to be explored. Thus, this topic aims to propose a combined reliability model to select the correct redundancy factor of DSCC-MMCC-based STATCOM.

Since the DSCC-MMCC redundancy factor selection considering both influence of constant and wear-out regions is still missing, this master thesis intends to fill this void. Therefore, the main goals of this work are listed:

- evaluate the dynamic behavior, reliability level and costs of DSCC-MMCC-based STATCOM design. Four voltage classes commercially available for Si devices are considered, covering the device blocking voltage capability range between 1.7 kV and 6.5 kV;
- DSCC-MMCC lifetime evaluation considering both wear-out and random failures data of the semiconductor devices.
- proposal of a flowchart for the redundancy factor design based on reliability requirements;
- proposal of a *reliability vs cost* map to evaluate the trade-off of different redundancy factor solutions.

The present research has been developed in the Centro Federal de Educação Tecnológica de Minas Gerais (CEFET-MG) in cooperation with the Gerência de Especialistas em Sistemas Elétricos de Potência (GESEP-UFV).

1.5 Master Thesis Outline

This master thesis is organized in 5 chapters as follows. Chapter 2 describes the modeling, control and design of the DSCC-MMCC-based STATCOM. The topology, control strategy, main parameters and components design are detailed. Additionally, dynamic behavior of different voltage classes in a DSCC-MMCC-based STATCOM are presented. In Chapter 3, the reliability model that combines both wear-out and random failures data of the semiconductor devices are presented. Chapter 4 describes the redundancy design based on reliability assessment. In addition, a reliability-based case study is conducted considering different redundancy factors for four device voltage classes in a DSCC-MMCC-based STATCOM. Finally, the conclusions of this work are stated in Chapter 5.

1.6 List of Publications

This master project has resulted in the publication of 3 journal papers and one conference paper. These publications are presented as follows:

1. J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. Seleme Jr. and R. Teodorescu, "On the Redundancy Strategies of Modular Multilevel Converters," in IEEE Transactions on Power Delivery, vol. 33, no. 2, pp. 851-860, April 2018. doi: 10.1109/TPWRD.2017.2713394.

2. J. V. M. Farias, A. F. Cupertino, V. N. Ferreira, S. I. Seleme Jr., H. A. Pereira and R. Teodorescu, "Design and lifetime analysis of a DSCC-MMC STATCOM," in proceedings of 2017 Brazilian Power Electronics Conference (COBEP), Juiz de Fora, 2017, pp. 1-6. doi: 10.1109/COBEP.2017.8257312.

3. J. V. M. Farias, A. F. Cupertino, V. N. Ferreira, H. A. Pereira, S. I. Seleme Jr. and R. Teodorescu, "Reliability-Oriented Design of Modular Multilevel Converters for Medium-Voltage STATCOM," in IEEE Transactions on Industrial Electronics, Early Access. doi: 10.1109/TIE.2019.2937050.

4. J. V. M. Farias, A. F. Cupertino, V. N. Ferreira, H. A. Pereira and S. I. Seleme Jr., "Redundancy Design for Modular Multilevel Converter based STATCOMs." in Microelectronics Reliability, In Press. doi: 10.1016/j.microrel.2019.113471.

The author also contributed to the following journal and conference publications in the topic of modular multilevel cascaded converters:

1. A. F. Cupertino, J. V. M. Farias, H. A. Pereira, S. I. Seleme Jr. and R. Teodorescu, "DSCC-MMC STATCOM Main Circuit Parameters Design considering Positive and Negative Sequence Compensation," in Journal of Control, Automation and Electrical Systems, v. 29, p. 62-74, February 2018, doi: 10.1007/s40313-017-0349-4.

2. A. F. Cupertino, J. V. M. Farias, H. A. Pereira, S. I. Seleme Jr. and R. Teodorescu, "Comparison of DSCC and SDBC Modular Multilevel Converters for STATCOM Application During Negative Sequence Compensation," in IEEE Transactions on Industrial Electronics, vol. 66, no. 3, pp. 2302-2312, March 2019. doi: 10.1109/TIE.2018.2811361.

3. P. R. Matias Jr., J. V. M. Farias, A. F. Cupertino, H. A. Pereira, M. M. Stopa and J. T. de Resende, "Redundancy and Derating Strategies for Modular Multilevel Converter for an Electric Drive." in Journal of Control, Automation and Electrical Systems, In Press.

4. P. R. Matias Jr., J. V. M. Farias, A. F. Cupertino, G. A. Mendonça, M. M. Stopa, H. A. Pereira "Selection of the Number of Levels of a Modular Multilevel Converter for an Electric Drive." 5th Southern Power Electronics Conference and 15th Brazilian Power Electronics Conference (COBEP), Santos, 2019.

5. R. O. de Sousa, J. V. M. Farias, A. F. Cupertino and H. A. Pereira, "Life consumption of a MMC-STATCOM supporting wind power plants: Impact of the modulation strategies." in Microelectronics Reliability. v. 88-90, p. 1063-1070, September 2018. doi: 10.1016/j.microrel.2018.06.111.

2 MMCC: Modeling, Control and Design

This chapter aims to present the topology, control and the main parameters design of the three-phase MMCC in double-star configuration based STATCOM. A case study considering 17 MVA/13.8 kV DSCC-MMCC-based STATCOM is conducted aiming to evaluate the dynamic response of the converter.

2.1 Topology and Control Design

The schematic of DSCC-MMCC is presented in Fig. 9. The converter is connected to the main grid through a grid inductance L_g and inductor resistance R_g. The grid inductance also includes the leakage inductance of the isolation transformer used when galvanic isolation is required. The six MMCC arms are composed of an inductor with inductance L_{arm} and resistance R_{arm}, k non-redundant cells and m redundant cells per arm. The total number of cells per arm is n, where $n = k + m$. All chopper cells consist of two IGBTs S_1 and S_2, two antiparallel connected diodes D_1 and D_2, and a capacitor C. Generally, there is a permanent bypass switch S_T (usually a thyristor) in parallel with each cell. In case of a cell failure, S_T bypasses the faulty cell (Gemmell et al., 2008). R_b represents the bleeder resistor, responsible for discharging the cell capacitor when the converter is turned off.

Assuming balanced capacitor voltages, sufficiently high switching frequency and high number of cells, the arm voltages v_u and v_l can be assumed as continuous variables, as presented in Fig. 10 (a). The DSCC-MMCC dynamics can be modeled based on the two equivalent circuits shown in Fig. 10 (b) and (c). The output current per phase can be obtained from Fig. 10 (b), based on Millman's theorem (Millman, 1940), as follows:

$$v_s - \left(\frac{1}{2}L_{arm} + L_g\right)\frac{di_g}{dt} - \left(\frac{1}{2}R_{arm} + R_g\right)i_g = v_g, \tag{2.1}$$

where v_g is the grid instantaneous line-to-neutral voltage and i_g is the grid current. The factor 1/2 appears in the arm inductance due to the Millman's theorem. v_s is the line-to-neutral voltage synthesized by the STATCOM (also referred to as output voltage), given by:

$$v_s = \frac{1}{2}(-v_u + v_l), \tag{2.2}$$

The control strategy is presented in Fig. 11. The proposed grid current control is responsible for injecting positive and negative sequence reactive power into the grid. This

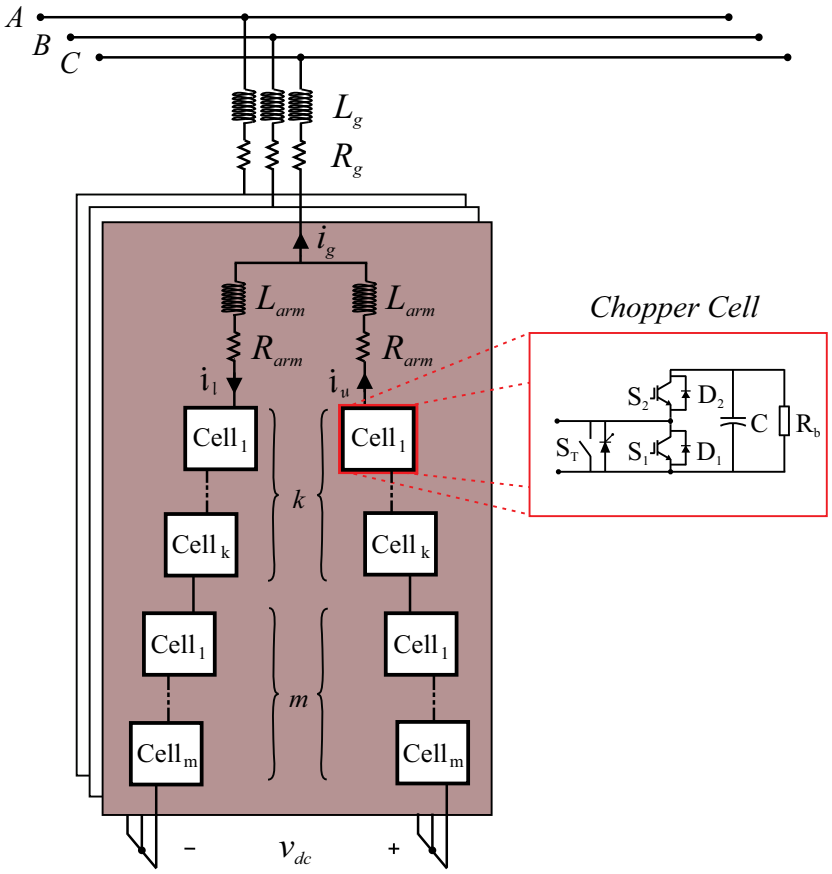

Figure 9 – Schematic of the DSCC-MMCC-based STATCOM.

control is implemented in stationary ($\alpha\beta$) reference frame. The external loop controls the square of the average voltage v_{avg} of all converter cells. The average voltage reference v^*_{avg} is dependent on the redundancy strategy employed. In this work, only active redundant cells are employed (Tu; Yang; Wang, 2019). The maximum number of "on-state" cells in each arm during a fundamental period is equal to k. Under such conditions, the total number of operating cells in the converter is $6k$. Therefore, the average voltage is computed by:

$$v_{avg} = \frac{1}{6k}\sum_{i=1}^{6k} v_{cell,i}, \tag{2.3}$$

where $v_{cell,i}$ is the ith cell voltage.

The average voltage reference v^*_{avg} is given by:

$$v^*_{avg} = \frac{v_{dc}}{k}, \tag{2.4}$$

where v_{dc} is the nominal MMCC dc-link voltage.

The average voltage loop calculates the necessary active power P^* exchanged with the grid. Using the instantaneous power theory (Akagi; Watanabe; Aredes, 2007), the grid

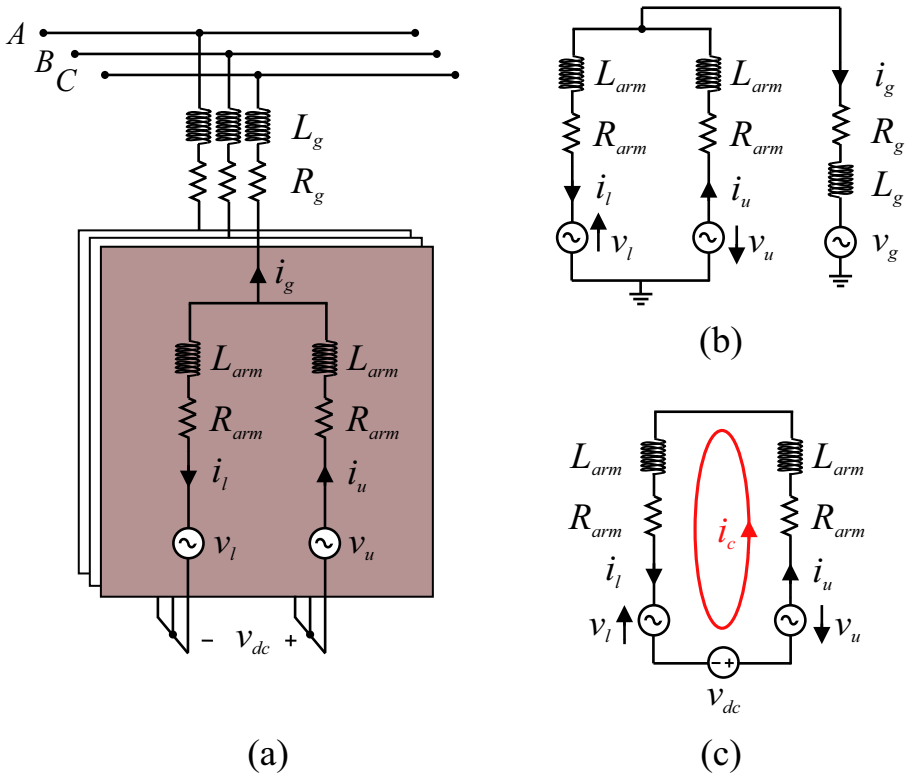

Figure 10 – Schematic of the DSCC-MMCC-based STATCOM: (a) Average model; (b) Equivalent circuit describing the output current dynamics; (c) Equivalent circuit describing the circulating current dynamics.

current reference can be computed by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = \frac{1}{v^2_{g\alpha} + v^2_{g\alpha}} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix}, \tag{2.5}$$

where $v_{g\alpha}$ and $v_{g\beta}$ are the stationary components of the grid voltage.

Proportional resonant (PR) controllers are employed to track the reference current. Applying the transformation from abc frame into the stationary ($\alpha\beta$) reference frame in Eq. (2.1), the dynamics of the grid current is given by:

$$v_{s,\alpha\beta} = v_{g,\alpha\beta} + L_{eq}\frac{di_{g,\alpha\beta}}{dt} + R_{eq}i_{g,\alpha\beta}, \tag{2.6}$$

where $L_{eq} = L_g + 0.5L_{arm}$, $R_{eq} = R_g + 0.5R_{arm}$ and $v_{s,\alpha\beta}$ is the equivalent output voltage of the MMCC. L_{arm} and R_{arm} are the inductance and the resistance of the arm inductors, respectively.

The circulating current control reduces the harmonics and inserts damping in the converter dynamic response. The circulating current dynamics can be obtained based on

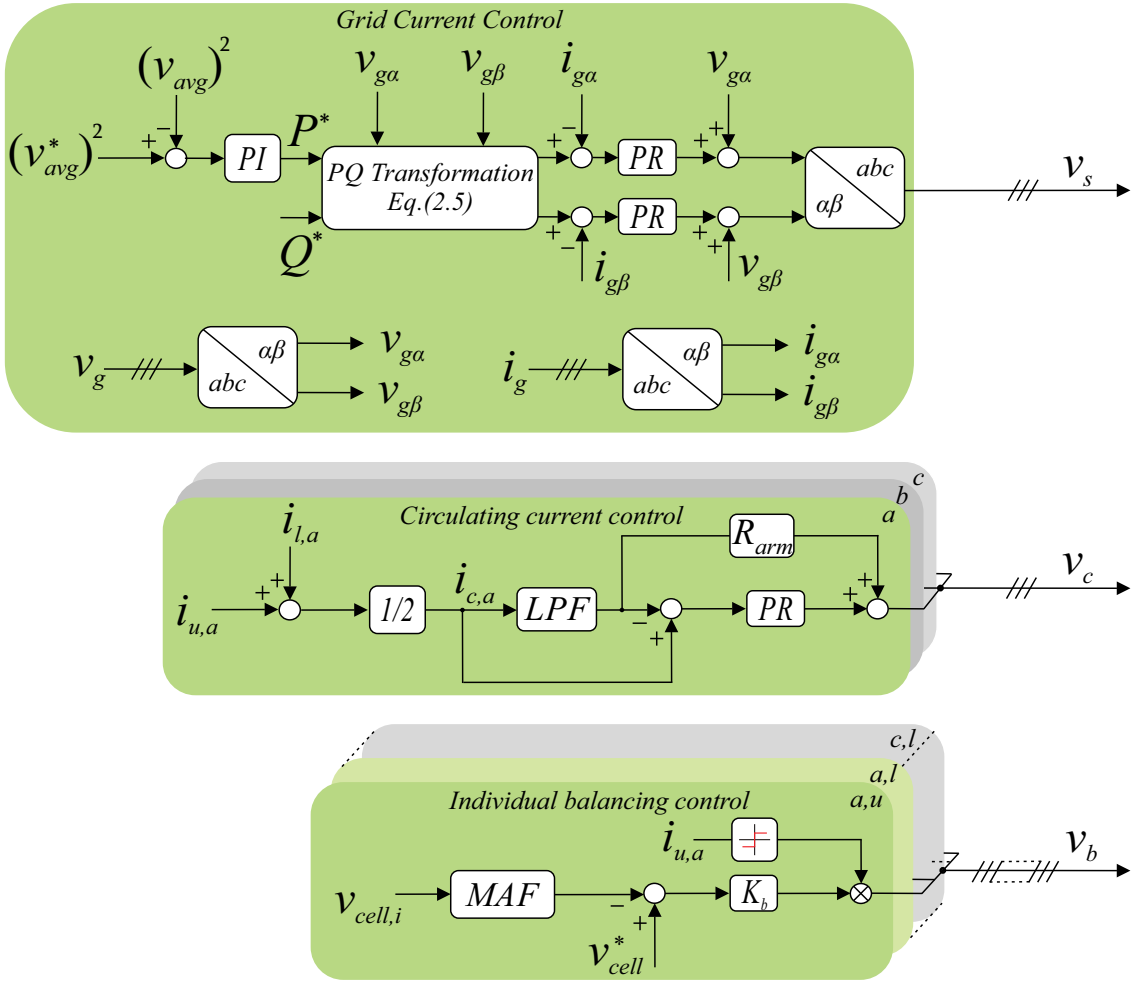

Figure 11 – Proposed control strategy for STATCOM.

Fig. 10 (c), as follows:

$$v_c + \frac{1}{2}v_{dc} - L_{arm}\frac{di_c}{dt} - R_{arm}i_c = 0, \tag{2.7}$$

where v_c is the STATCOM internal voltage (which drives the circulating current) given by:

$$v_c = -\frac{1}{2}(v_u + v_l), \tag{2.8}$$

and i_c is the converter circulating current giving by:

$$i_c = \frac{i_u + i_l}{2}. \tag{2.9}$$

where i_u and i_l are the upper and lower arm currents, respectively.

Figure 11 presents the circulating current control loop. The circulating current reference i_c^* is obtained through low-pass filtering of i_c (Harnefors et al., 2013). A butterworth second-order filter is employed. Furthermore, according to Xu et al. (2016), a

considerable 2nd harmonic component is present in the circulating current. This second order component generally cannot be compensated by the proportional controller (Yue et al., 2016). In view of this problem, a resonant controller tuned to the 2nd harmonic is added to the circulating current control.

This paper uses the phase-shift carrier pulse width modulation (PSC-PWM) method with injection of 1/6 of third harmonic in the phase voltages (Ilves et al., 2014). The angular displacement of the carriers is calculated by the following equation:

$$\theta_{u,n} = 2\pi\left(\frac{l-1}{n}\right) \quad and \quad \theta_{l,n} = \theta_{u,n} + \beta_c,$$

where $l = 1, 2, ..., n$. The angle β_c indicates the angular displacement between the carrier waveforms in the upper and lower arms.

Regarding PSC-PWM angular displacement, $(k+1)$ level and $(2k+1)$ level modulation strategies can be chosen in terms of the desired harmonic performance (Ilves et al., 2013). As observed in Fig. 12, the DSCC-MMCC output voltage has more levels in the $(2k+1)$ level modulation. This fact provides to the $(2k+1)$ level modulation a superior performance in terms of power quality at the ac side. Since in STATCOM applications the ac side power quality is preferred, the $(2k+1)$ level modulation is employed (Sasongko et al., 2016). The angular displacement is given by:

$$\beta_c = 0 \quad \text{, k is odd} \qquad \beta_c = \frac{\pi}{k} \quad \text{, k is even}$$

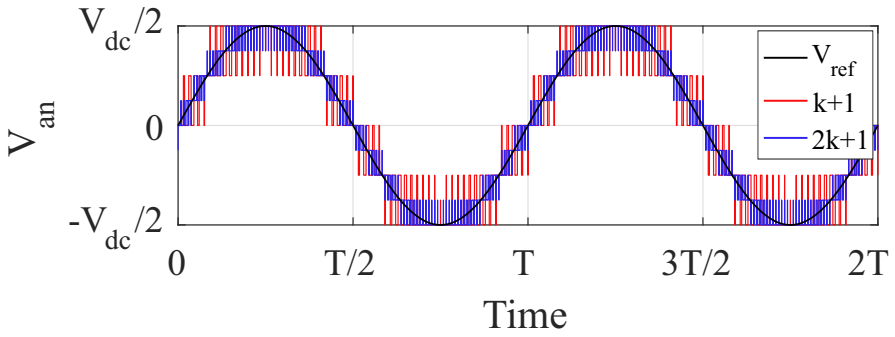

Figure 12 – DSCC-MMCC output voltage comparison of $(k+1)$ level and $(2k+1)$ level phase-shifted modulation schemes. *Remark*: k = 4 cells per arm.

In the PSC-PWM method, an extra individual balancing control loop is necessary, as observed in Fig. 11. As suggested by Hagiwara and Akagi (2009), a proportional controller k_b is employed. In this case, the individual balancing control law is given by:

$$v_b = k_b(v^*_{cell} - v_{cellf,i})sign(i_{cell,i}), \tag{2.10}$$

where $i_{cell,i}$ is the arm current of the ith cell. $v_{cellf,i}$ is obtained from the individual capacitor voltages through a moving average filter (Sasongko et al., 2016). The reference voltages v_s, v_c and v_b are inputs of the modulation strategy as illustrated in Fig. 13. Under such conditions, the normalized reference signals per phase are given by:

$$v_{u,n} = v_b + \frac{v_c}{v^*_{cell}} - \frac{v_s}{kv^*_{cell}} + \frac{1}{2}, \tag{2.11}$$

$$v_{l,n} = v_b + \frac{v_c}{v^*_{cell}} + \frac{v_s}{kv^*_{cell}} + \frac{1}{2}. \tag{2.12}$$

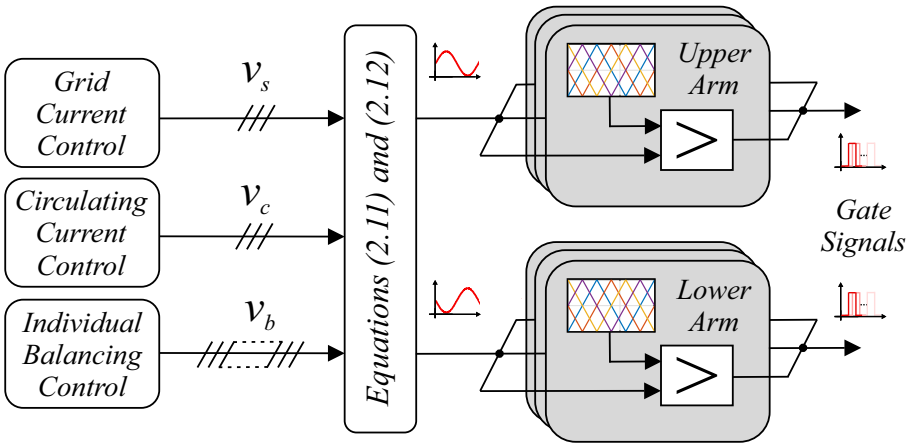

Figure 13 – Connection between the control and the modulation scheme.

2.2 DSCC-MMCC-based STATCOM Design

2.2.1 Switching Frequency

In MMCC applications, the switching and sampling frequencies are important issues (Siddique et al., 2016). Since the double-star configuration and PSC-PWM modulation are employed, a total number of carriers required in a period of the grid voltage is $2k$. Therefore, the effective output frequency is given by (Marzoughi; Burgos; Boroyevich, 2019):

$$f_{ef} = 2kf_c, \tag{2.13}$$

where f_c is the carrier frequency of each MMCC cell. Sasongko et al. (2016) discuss the stability of the DSCC-MMCC capacitor voltage balancing for various values of f_c. The presented analysis shows that interesting values for switching frequency are 5/2 times, 7/2 times or 4 times the line frequency. The first value results in minimum losses, while the last results in better dynamic performance and capacitor voltage balancing. Nevertheless, Ilves et al. (2015) show switching frequencies integer multiple of the line frequency may

cause instability in the capacitor voltage balancing. Therefore, $f_c = 210\ Hz$ is employed in this work, which corresponds to 7/2 times the line frequency (60 Hz).

Since the ac component included in cell capacitor voltages works as a disturbance in the current control system, it should be eliminated by a moving-average filter (Sasongko et al., 2016), the window time must be:

$$1/f_{ma} = f'_n/f_n, \tag{2.14}$$

where f'_n is obtained from the irreducible fraction of the carrier frequency f_c with respect to the supply frequency f_n, denoted by f'_c/f'_n. [1]

2.2.2 Number of Cells

The following considerations are assumed to evaluate the DSCC-MMCC number of cells:

- The variations in the grid voltage $V_g = 13.8$ kV are assumed ± 5%;
- The STATCOM output impedance in pu is considered 14% with a variation of ± 5%;
- The dc-link voltage v_{dc} presents in the worst case 10% of ripple and a constant error of 3% in steady-state;
- Converter design considering both positive and negative sequence current compensation.

Under these conditions, the effective line-to-line voltage synthesized by the STATCOM V_s must be given by (Cupertino et al., 2019):

$$V_s \approx 1.2V_g, \tag{2.15}$$

where V_g is the PCC effective line-to-line voltage.

The minimum value of the dc-link voltage can be approximated by (Fujii; Schwarzer; De Doncker, 2005):

$$v_{dc} = \frac{2\sqrt{2}}{0.87\sqrt{3}} \frac{V_s}{m_{i,max}}, \tag{2.16}$$

[1] For example, when $f_c = 210$ Hz and $f_n = 60$ Hz, $f'_c/f'_n = 7/2$. Therefore, $f'_c = 7$ and $f'_n = 2$. Thereby, $1/f_{ma} = 2/f_n$.

where $m_i = 2\hat{V}/v_{dc}$ is the modulation index and $\hat{V}$ is the peak value of phase voltage. The maximum modulation with the injection of 1/6 of third harmonic is $m_{i,max} = 1.15$. Therefore, the approximate value of the effective dc-link voltage is $v_{dc} = 28$ kV.

The number of non-redundant cells is determined by:

$$k = \frac{1}{f_{us}} \frac{V_{dc}}{V_{svc}}, \tag{2.17}$$

where f_{us} is the device utilization factor defined by the ratio between the reference voltage of cells v^*_{cell} and the semiconductor device voltage class V_{svc}. Table 4 indicates typical values for device utilization factor based on failure rate for one IGBT module (ABB, 2017). Failure rate depend on the operating conditions such as blocking voltage utilization, and altitude above sea level due to increased cosmic ray activity (Huber; Kolar, 2017). A typical failure rates for one IGBT module is 100 failure in time (FIT). As observed, the maximum recommended nominal voltage for semiconductor devices are below 60% of V_{svc}. Therefore, assuming a cell capacitor voltage ripple of up to 10%, $f_{us} = 50\%$ is employed in this work. Finally, a higher number of cells per arm is required to achieve the value of the dc-link voltage, when semiconductor devices with lower blocking voltage are employed.

Table 4 – IGBT modules specifications for DSCC-MMCC.

$\mathbf{V}_{svc}$ (V)	$\mathbf{V}_{@100FIT}$ (V)	$\mathbf{f}_{us}(\%)$
1700	900	52.94
3300	1800	50.00
4500	2250	50.00
6500	3600	55.38

2.2.3 Current Ratings

2.2.3.1 Arm Currents

Expressions for the DSCC-MMCC arm currents can be used to define the current of the semiconductor devices. Arm currents per phase can be expressed by:

$$i_u = i_c + \frac{i_g}{2}, \tag{2.18}$$

$$i_l = i_c - \frac{i_g}{2}. \tag{2.19}$$

If the MMCC injects both positive and negative sequence currents, i_g is given by:

$$i_g = \widehat{I}_n^+ cos(\omega t + \phi^+ + \theta_v) + \widehat{I}_n^- cos(\omega t + \phi^- - \theta_v), \tag{2.20}$$

where $\theta_v \in \{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\}$ refers to the phase angle of each phase and ϕ is the phase difference between grid voltage and current. Considering that the harmonics in the circulating current are suppressed, its value can be given by:

$$i_c = \frac{m_i}{4}\widehat{I}_n^+ cos(\phi^+) + \frac{m_i}{4}\widehat{I}_n^- cos(\phi^- + \theta_v), \tag{2.21}$$

Due to symmetry, only the upper arm current is verified. The maximum value for the current is given by:

$$\max(i_u) = \max(i_c) + \frac{1}{2}\max(i_g). \tag{2.22}$$

According to (Yue et al., 2016), $\max(i_c) \leq \frac{1}{4} m_{i,max}\widehat{I}_n$ and $\max(i_g) \leq \widehat{I}_n$, where $\widehat{I}_n$ is given by:

$$\widehat{I}_n = \frac{\sqrt{2}}{\sqrt{3}}\frac{S_n}{V_g}. \tag{2.23}$$

Thus, the maximum and rms upper arm current are:

$$max(i_u) = \left(\frac{1}{2} + \frac{m_{i,max}}{4}\right)\widehat{I}_n, \tag{2.24}$$

$$i_{u,rms} = \frac{\widehat{I}_n}{2}\sqrt{\frac{(\lambda m_{i,max})^2}{4} + \frac{1}{2}}. \tag{2.25}$$

Considering $m_{i,max} = 1.15$, the maximum and rms upper arm current values are $max(i_u) = 0.79\widehat{I}_n$ and $i_{u,rms} = 0.46\widehat{I}_n$, respectively.

2.2.3.2 Current Efforts in Semiconductors Devices

Current efforts can be evaluated for a suitable design of semiconductor devices. Due to symmetry, only the upper arm is analyzed. Considering $i_u > 0$, the devices capable of conducting are S_2 and D_1. According to Sousa (2014), the average currents flowing through the semiconductors devices S_2 and D_1 of one cell are given by:

$$i_{S_2,avg} = \frac{1}{2\pi}\left(\int_0^{\theta_{z,1}} m_u i_u d\omega t + \int_{\theta_{z,2}}^{2\pi} m_u i_u d\omega t)\right), \tag{2.26}$$

$$i_{D_1,avg} = \frac{1}{2\pi}\left(\int_0^{\theta_{z,1}} \overline{m}_u i_u d\omega t + \int_{\theta_{z,2}}^{2\pi} \overline{m}_u i_u d\omega t\right). \tag{2.27}$$

where $\theta_{z,1}$ and $\theta_{z,2}$ are angles that define the zero crossing of the current arm, m_u is the ideal modulation signal of upper arm and $\overline{m}_u = 1 - m_u$. The angles $\theta_{z,1}$ and $\theta_{z,2}$ are described by (Sousa, 2014):

$$\theta_{z,1} = \pi - \phi - cos^{-1}\left(\frac{m_i cos(\phi)}{2}\right), \tag{2.28}$$

$$\theta_{z,2} = \pi - \phi + cos^{-1}\left(\frac{m_i cos(\phi)}{2}\right). \tag{2.29}$$

In the STATCOM operation mode, the phase difference between grid voltage and current is equal to $\phi = \pm\frac{\pi}{2}$. Thus, Eqs. (2.28 and 2.29) can be described by:

$$\theta_{z,1} = \begin{cases} 0 & if,\ \phi = \frac{\pi}{2} \\ \pi & if,\ \phi = -\frac{\pi}{2}, \end{cases}, \tag{2.30}$$

$$\theta_{z,2} = \begin{cases} \pi & if,\ \phi = \frac{\pi}{2} \\ 2\pi & if,\ \phi = -\frac{\pi}{2}, \end{cases}. \tag{2.31}$$

In addition, with injection of 1/6 of third harmonic in the phase voltages, the ideal modulating signal of the upper arm is given by:

$$m_u = \frac{1}{2} - \frac{m_i}{2} cos(\omega t) + \frac{m_i}{12} cos(3\omega t). \tag{2.32}$$

When $i_u < 0$, the average current in S_1 and D_2 can be calculated by:

$$i_{S_1,avg} = \frac{1}{2\pi}\int_{\theta_{z,1}}^{\theta_{z,2}} -\overline{m}_u i_u d\omega t, \tag{2.33}$$

$$i_{D_2,avg} = \frac{1}{2\pi}\int_{\theta_{z,1}}^{\theta_{z,2}} -m_u i_u d\omega t. \tag{2.34}$$

Considering only positive sequence currents injection and $i_c = 0$ in STATCOM operation mode, the average currents in the semiconductor devices are given by:

$$i_{S_1,avg} = i_{S_2,avg} = i_{D_1,avg} = i_{D_2,avg} = \frac{\widehat{I}_n}{4\pi}. \tag{2.35}$$

Assuming that the power losses are evenly distributed among each cells of arm, Eq. (2.35) can be considered the average current in S_1, S_2, D_1 and D_2 of any upper arm cell.

The rms currents of the devices can be evaluated by:

$$i_{S_2,rms} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\theta_{z,1}} m_u i_u^2 d\omega t + \int_{\theta_{z,2}}^{2\pi} m_u i_u^2 d\omega t)\right)}, \tag{2.36}$$

$$i_{D_1,rms} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\theta_{z,1}} \overline{m}_u i_u^2 d\omega t + \int_{\theta_{z,2}}^{2\pi} \overline{m}_u i_u^2 d\omega t\right)}, \tag{2.37}$$

$$i_{S_1,rms} = \sqrt{\frac{1}{2\pi}\int_{\theta_{z,1}}^{\theta_{z,2}} -\overline{m}_u i_u^2 d\omega t}, \tag{2.38}$$

$$i_{D_2,rms} = \sqrt{\frac{1}{2\pi}\int_{\theta_{z,1}}^{\theta_{z,2}} -m_u i_u^2 d\omega t}. \tag{2.39}$$

Under such conditions, the rms currents in the semiconductor devices are given by:

$$i_{S_1,rms} = i_{S_2,rms} = i_{D_1,rms} = i_{D_2,rms} = \frac{\widehat{I}_n}{4\sqrt{2}}, \tag{2.40}$$

It is notable that the rms upper arm current in Eq. (2.24) is higher than rms currents in the semiconductor devices ($0.46\widehat{I}_n > \frac{1}{4\sqrt{2}}\widehat{I}_n$). For this reason, the nominal current of the devices will be chosen through Eq. (2.24), in this work.

2.2.4 Cell Capacitance and Arm Inductance

The cell capacitance can be designed based on the converter energy storage requirements. According to (Ilves et al., 2014), the minimum cell capacitance is given by:

$$C = \frac{kS_n W_{conv}}{3v_{dc}^2}, \tag{2.41}$$

where W_{conv} is the required energy storage per MVA. The minimum required value of W_{conv} is approximately 40 kJ/MVA, as defined in (Farias et al., 2018).

Regarding the arm inductance, some papers present methodologies based on DSCC-MMCC circulating current. Once the control strategy suppresses the second harmonic component of the circulating current, the following relationship must be satisfied to prevent the resonance frequency (Ilves et al., 2012):

$$L_{arm}C > \frac{5k}{48\omega_n^2}. \tag{2.42}$$

Another feature performed by the inductor is to limit the arm current during faults (Xu; Xiao; Zhang, 2016). Considering a short circuit applied between the positive and negative dc-buses, the arm inductance which limits the fault current is calculated by:

$$L_{arm} = \frac{v_{dc}}{2\alpha}, \tag{2.43}$$

where α (kA/s) is the maximum current rise rate.

To limit the peak-to-peak circulating current ripple Δi_c for STATCOM application, the arm inductance can be computed as follows (Li; Jones; Wang, 2017):

$$L_{arm} = \frac{3}{32C\omega_n f_c}\frac{\widehat{I}_n}{\Delta i_c}, \tag{2.44}$$

In this work, the arm inductors are designed to satisfy the above constraint and to limit the total harmonic distortion (THD) in output current i_g below 5% (IEEE, 2014). Moreover, the maximum peak-to-peak circulating current ripple $\Delta i_c = 2\%$ is applied. The grid impedance is considered unchanged.

2.3 Steady-State Performance Evaluation

2.3.1 Case Study

A 17 MVA MMCC-STATCOM with effective line-to-line voltage of 13.8 kV at the point of common coupling (PCC) is considered. Table 5 presents the main circuit parameters. Based on the topology presented in Fig. 9, the simulations were performed using PLECS software aiming to evaluate the DSCC-MMCC dynamic and steady-state performance.

Table 5 – Main parameters of the MMCC for four proposed designs.

Parameter		**MMCC specifications**			
		C_{17}	C_{33}	C_{45}	C_{65}
k		33	17	13	9
v_{dc}	(kV)	28	28	28	28
V_{svc}	(kV)	1.7	3.3	4.5	6.5
V^*_{cell}	(kV)	0.85	1.65	2.15	3.11
$i_{arm,rms}$	(A)	460	460	460	460
$\widehat{I}_{arm}$	(A)	788	788	788	788
C	(mF)	9.54	4.92	3.76	2.61
L_{arm}	(mH)	4.46	8.70	11.82	17.08
L_g	(mH)	1.5	1.5	1.5	1.5
f_c	(Hz)	210	210	210	210
f_{ef}	(kHz)	6.93	3.57	2.73	1.89

The controller parameters are shown in Tab. 6. The proportional integral controllers are discretized by Tustin method (Ukakimaparn et al., 2018), while the proportional resonant controllers are discretized by Tustin with prewarping method.

The proposed case study considers only positive sequence injection. Under such conditions, the trapezoidal reactive power profile presented in Fig. 14 is employed. The aim is to verify if the performance of the capacitor voltage balancing and if the selected parameters are suitable for the inductive and capacitive operation.

Table 6 – DSCC-MMCC-based STATCOM parameters of the controller.

Parameter	C_{17}	C_{33}	C_{45}	C_{65}
Proportional gain of average control ($\Omega^{-}1$)	32.6	8.7	5.1	2.4
Integral gain of average control ($\Omega^{-}1/s$)	559	148	87	42
Proportional gain of grid current control (Ω)	32	26	25	23
Resonant gain of grid current control (Ω/s)	1000	1000	1000	1000
Proportional gain of circulating current control (Ω)	1.2	2.4	3.2	4.6
Resonant gain of circulating current control (Ω/s)	1000	1000	1000	1000
Circulating current LPF cut-off frequency (Hz)	8	8	8	8
Proportional gain of individual balancing control ($V^{-}1$)	0.0004	0.0004	0.0004	0.0004

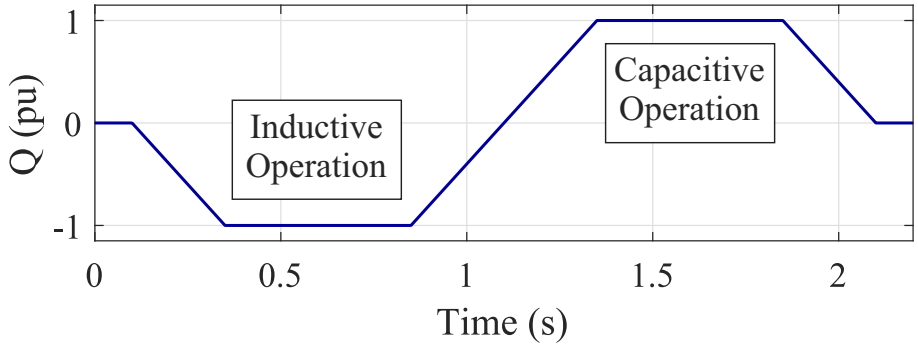

Figure 14 – Reactive power profile considering both inductive and capacitive operation.

2.3.2 Results

The instantaneous active and reactive powers are presented in Fig. 15. As observed, the reactive power exchanged follows the reference profile. Furthermore, the active power presents a low average value corresponding to the converter losses.

The grid currents shown in Fig. 16 presents the same shape of reactive power. Additionally, Table 7 summarizes the THD for all cases in both inductive and capacitive operation. As observed, the C_{65} design presents higher grid current distortion with $THD = 0.62\%$ and $THD = 0.81\%$ for inductive and capacitive operation, respectively. Furthermore, all designs meet the THD limit on the i_g output current of 5%.

Table 7 – THD comparison for all cases in two different operating modes.

Parameter	Operation	C_{17}	C_{33}	C_{45}	C_{65}
THD (%)	Inductive	0.22	0.46	0.51	0.62
	Capacitive	0.26	0.52	0.59	0.81

The circulating currents are presented in Fig. 17. As observed, a reduction in the number of output voltage levels of the converter results in an increase in the circulating current ripple. Figure 17 (d) shows that the largest ripple of circulating current happens in the C_{65} design. Nevertheless, all designs present Δi_c values below 2% as specified at the design stage.

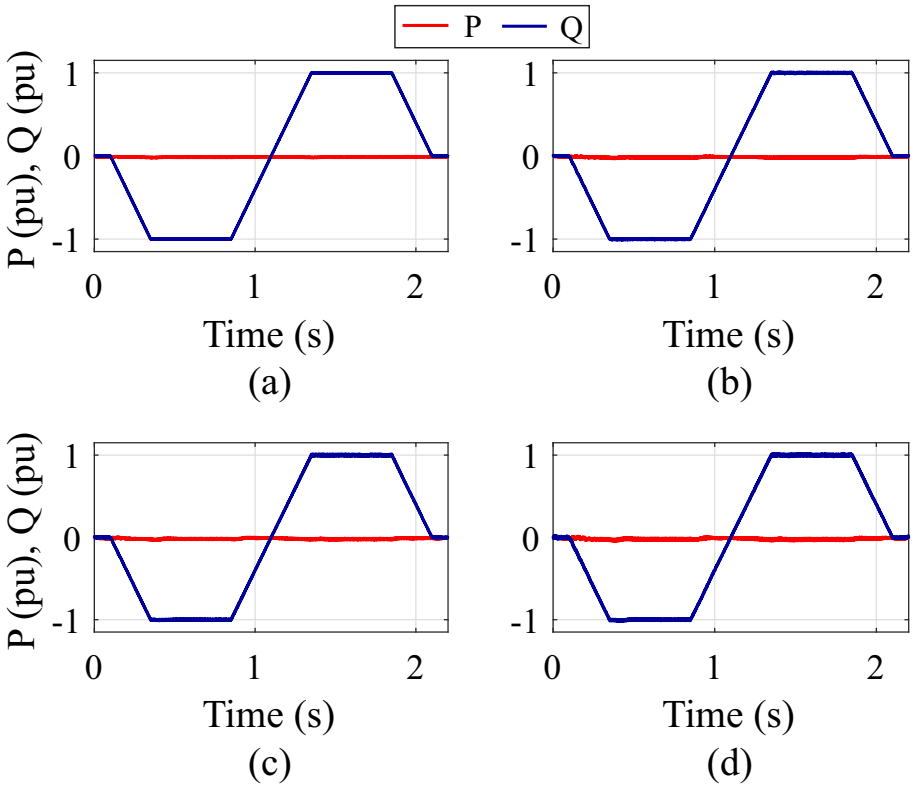

Figure 15 – Instantaneous active and reactive power of DSCC-MMCC: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}

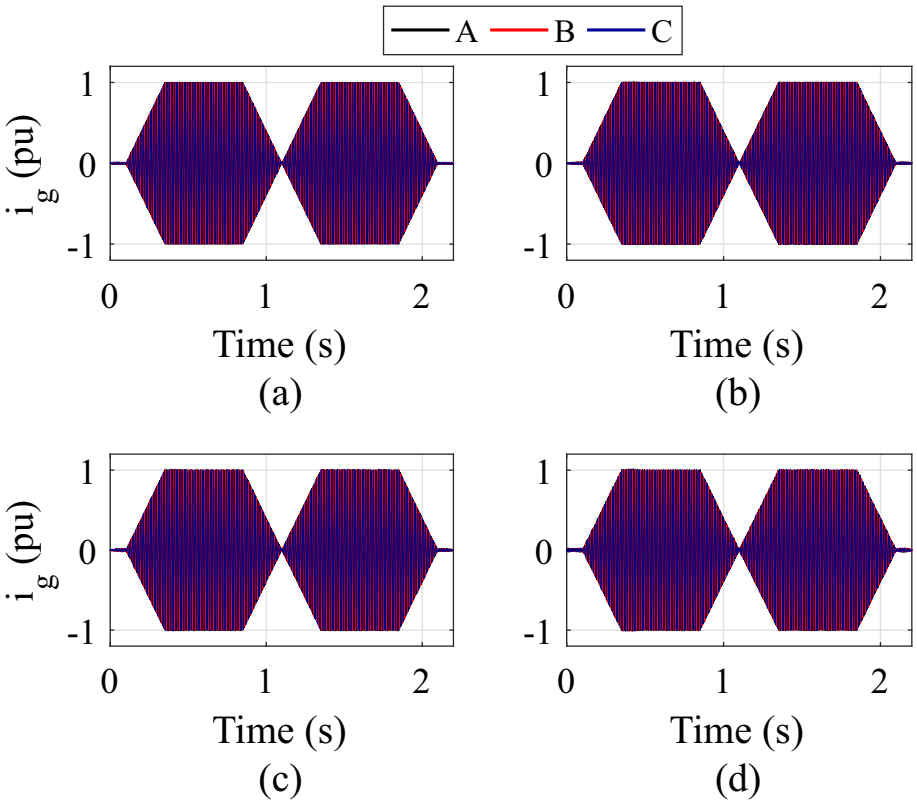

Figure 16 – Grid currents dynamic behavior of DSCC-MMCC: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}

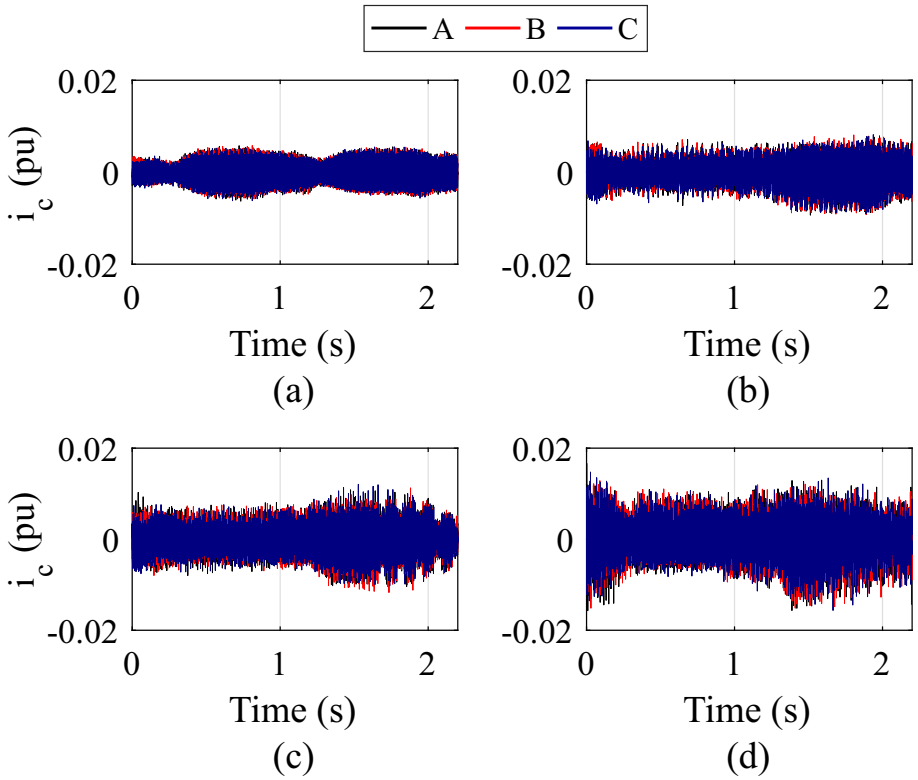

Figure 17 – DSCC-MMCC circulating currents: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

The cell voltages for the upper arm of phase A are presented in Fig. 18. The blue dashed lines indicate the 10% tolerance band adopted in the capacitance design. As observed, during the inductive operation, the capacitor voltage $v_{cell,i}$ waveforms present values smaller than the lower tolerance band. An analogous phenomenon is observed in the upper tolerance band during capacitive operation. Indeed, the energy storage requirements previously derived assume all capacitor voltages are perfectly balanced. Therefore, the average value of capacitor voltages v_{avg} is within the tolerance band limits.

Additionally, Figs 19 and 20 present in detail the behavior of $v_{cell,i}$ and v_{avg} for inductive and capacitive operation, respectively. As observed, there is a spread in the cell capacitors voltages for all cases. Moreover, a larger number of cells accentuate the spread in both inductive and capacitive operation.

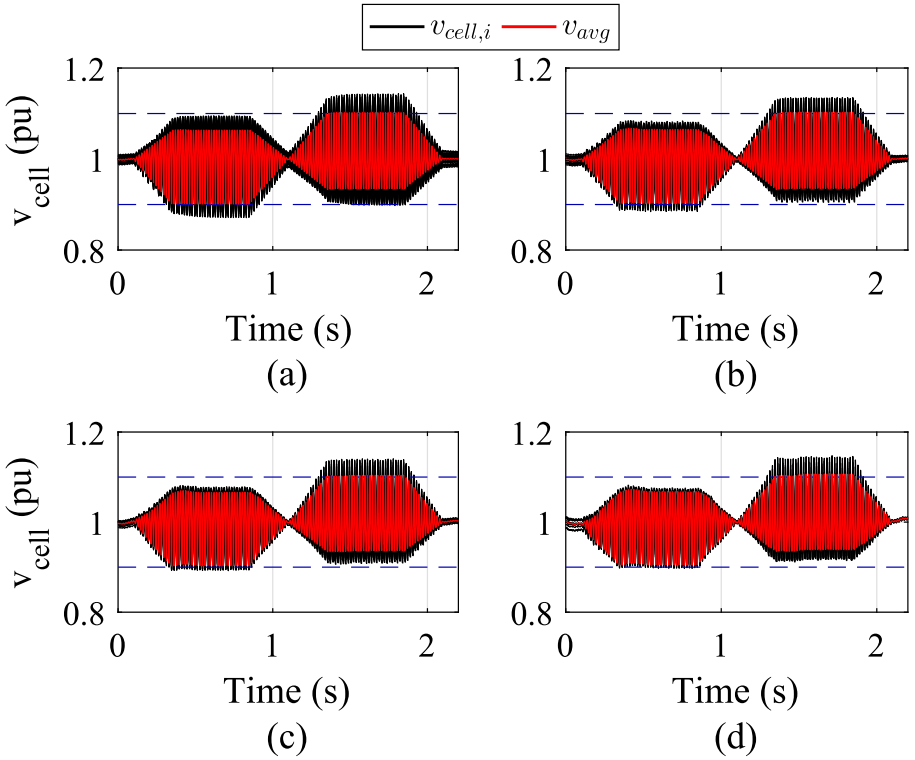

Figure 18 – DSCC-MMCC cell voltages in the upper arm of phase A: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

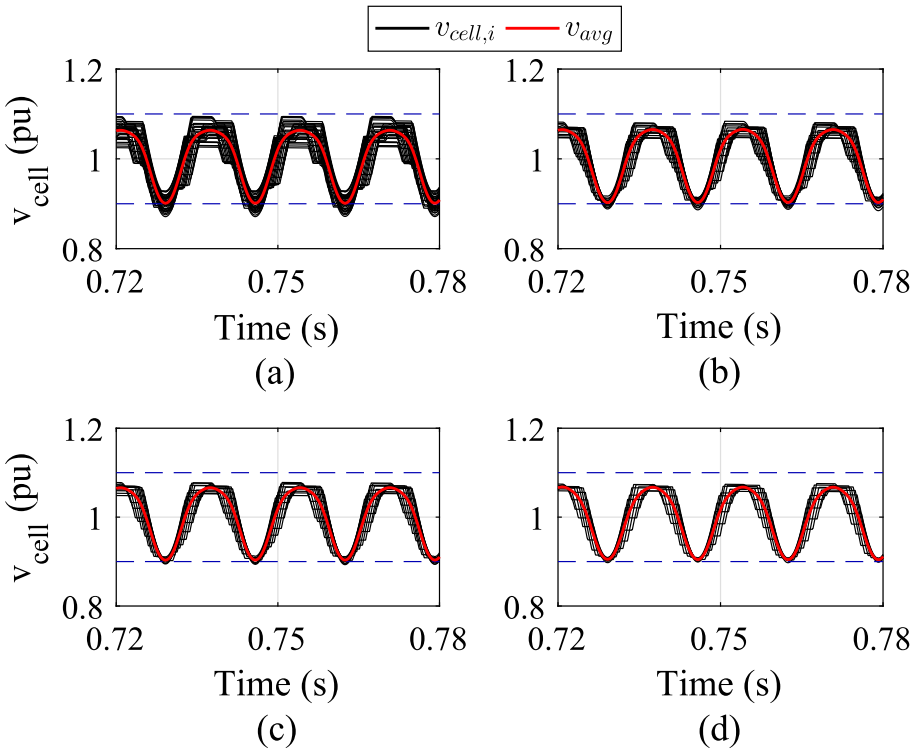

Figure 19 – DSCC-MMCC cell voltages detail in the upper arm of phase A for inductive operation: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

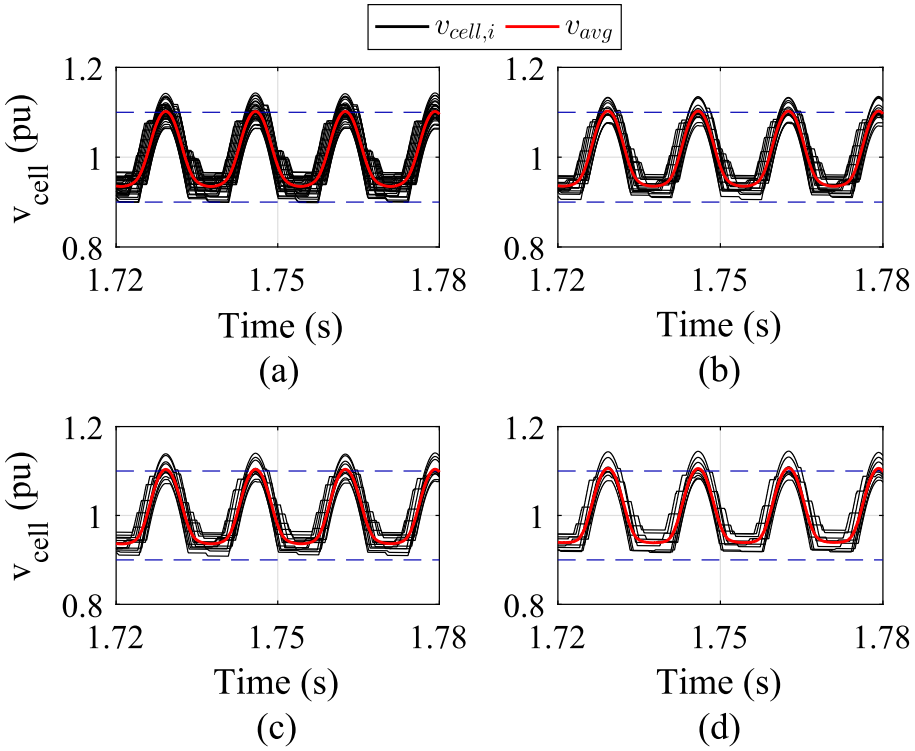

Figure 20 – DSCC-MMCC cell voltages detail in the upper arm of phase A for capacitive operation: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

2.4 Chapter Conclusions

In this chapter the topology, control and design of DSCC-MMCC-based STATCOM were presented. In addition, the dynamic response of the converter was analyzed for four different voltage class designs. The results shown satisfactory response of reactive power, grid current and circulating current, demonstrating effectiveness of the controls employed.

Although the four voltage classes presented similar results in terms of dynamic performance, these designs present different number of components. Therefore, the designs differ in terms of reliability. Next chapter discusses a reliability-oriented design for DSCC-MMCC-based STATCOMs.

3 Reliability Modeling of a DSCC-MMCC-Based STATCOM

Power electronic systems play an increasingly important role in providing high efficiency power conversion. However, they are often presented with demanding operating environments that challenge their reliability (Baker et al., 2014). Depending on the application of a specific system, a number of stressors (e.g., high temperatures, temperature cycling, humidity, dust, vibration, electromagnetic interference (EMI), and radiation) can remove the component from safe operation zone. The large number of fragile elements in power electronics systems include semiconductors, capacitors, magnetics, controllers, sensors, and auxiliary devices. The failure of a single part can cause downtime and maintenance cost. The need for dependable systems forces both academia and industry to pursue advances in reliability research (Wang et al., 2014).

In general definition, reliability is the probability that a device will perform its intended working for a specified period of time under normal operation (Richardeau; Pham, 2013; IEEE, 2009). There are many reasons that can lead a device to failure. Since the risk of failures cannot be fully eliminated, they should be reduced to tolerable levels (Ferreira; Filho; Rocha, 2017). Some reasons that can lead to device failure are:

- *overstress*: is related to a single phenomenon (e.g., overvoltage or overload), when product capacities are exceeded.
- *wear-out*: is related to cumulative damage and aging process of the devices.
- *inherent design features*: the potential for failure is related with the project complexity.
- *error*: installation errors, improper maintenance and inappropriate use are examples of failures caused by errors.

In recent years, the energy and industry segments have brought high reliability requirements for power electronic converters. In such application fields, the cost of a single failure can result in considerable financial losses. Furthermore, the critical industrial applications and harsh environmental conditions are important factors which drive studies regarding reliability in power electronic systems (Wang; Liserre; Blaabjerg, 2013).

Industry experience classifies semiconductor power devices as the most fragile component of power electronic converters (Yang et al., 2011). Besides, many industry survey participants define power semiconductors as the most crucial elements to be researched to improve the power converter reliability (Falck et al., 2018).

3.1 Basics of Reliability Modeling

In view of the aforementioned reliability concerns, possible solutions to improve the reliability of power electronic converters can be cited such as, Design for Reliability (DFR), redundancy strategies, junction temperature control and fault-tolerant topologies (Wang; Ma; Blaabjerg, 2012; Ghimire et al., 2014; Sintamarean et al., 2015; Blaabjerg et al., 2017; Tu; Yang; Wang, 2019).

Two important tools for reliability modeling are the reliability function $R(x)$ and failure rate $\lambda(x)$. $R(x)$ is defined as the probability that a device will perform its intended work for a specified period of time under normal operation where the device works within its safe operating area (Richardeau; Pham, 2013). $R(x)$ is given by (Todinov, 2007):

$$R(x) = 1 - F(x) = \frac{N(x)}{N(0)}, \tag{3.1}$$

where $N(x)$ is the number of surviving devices at time x and $N(0)$ is the number of devices at the initial time. $F(x)$ is the unreliability function of the device.

The failure rate function denoted by $\lambda(x)$ is defined as the probability that a device will fail in the next time unit given that it has been working properly up to time x, i.e. (Todinov, 2007):

$$\lambda(x) = \lim \frac{N(x) - N(x + \Delta x)}{N(0)\Delta x}. \tag{3.2}$$

The relation between the failure rate $\lambda(x)$ and $R(x)$ is given by (Richardeau; Pham, 2013):

$$\lambda(x) = -\frac{1}{R(x)} \frac{dR(x)}{dx}. \tag{3.3}$$

A typical failure rate curve of a power electronics product (also called bathtub curve) is plotted in Fig. 21. The device failure rate is usually characterized by three regions: early failure period, constant failure rate and wear-out period. The early failure period is defined by manufacturing constraints and it is infeasible to deal with it in the application level. The period where a constant device failure rate occurs is often referred to as the useful life of the device. The wear-out period is often called the aging failure period due to electro-thermo-mechanical stress and wear-out of the packaging of the semiconductor device. The lifetime of the device is close to its end once it enters this period, unless there is preventive maintenance or a major derating of the operation (Richardeau; Pham, 2013).

It should be noticed that the constant failure rate is used in the converter design, while preventative maintenance and replacement schedules are considered in wear-out phase

(Tu; Yang; Wang, 2019). Since the constant failure region and wear-out period depend on failure events and system behavior, the reliability-based strategies can be applied to control the failure rate and to ensure continuity of service during a target lifetime.

Some works propose a DFR approach as a solution to ensure a target lifetime for the power converters (Blaabjerg et al., 2017). In this concept, the design is accomplished to avoid the system to move forward to the wear-out zone. As a result, the probability of wear-out failures can be reduced during the design phase. Although the wear-out failures can be predicted (to some extent) and even avoided, the catastrophic/random failure are more difficult to predict (Iannuzzo, 2016). In the next sections, the reliability modeling of a DSCC-MMCC in both failure regions is described.

3.2 Constant Failure Region

In the constant failure region, except for pulse mode or thermal/power cycling mode, electronic devices have a very long useful life period so the failure rate is constant and equal to λ in Fig. 21. Thus, considering the differential equation described through Eq. (3.3) and including a constant failure rate $\lambda(x) = \lambda$ the general reliability law and modeling is:

$$R(x) = e^{-\lambda x}. \tag{3.4}$$

Firstly, the reliability of semiconductor devices must be computed using Eq. (3.4). A standard power module (IGBT with anti-parallel diode) is considered. The IGBT module failure rate is constant and equal to λ_{IGBT}. Thus, the module reliability is described by:

$$R_{IGBT,cf}(x) = e^{-\lambda_{IGBT} x}, \tag{3.5}$$

The failure rate depends on the technological complexity of the devices and some factors that can be included in the λ_{IGBT} formulation as given by (Department of Defense

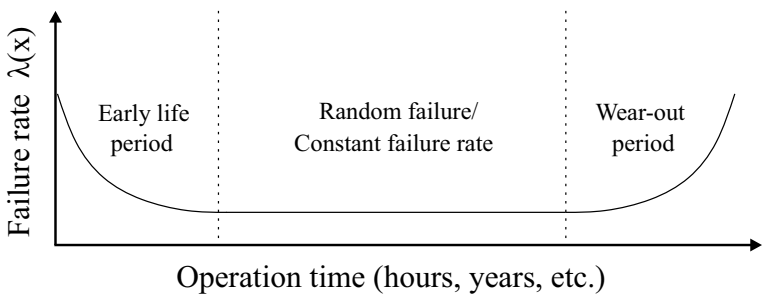

Figure 21 – Typical failure rate curve - bathtub curve.

- USA, 1998):

$$\lambda_{IGBT} = \lambda_b \pi_T \pi_S \pi_E \pi_A, \tag{3.6}$$

where λ_b is the component base failure rate, π_T is the temperature factor, π_S is the electric stress factor, π_E environmental factor and π_A is the application factor. Base failure rate is defined at junction temperature of $T_j = 100°$ C, which depends on the technological class of the devices and package. According to Richardeau and Pham (2013), λ_b is equal to 50 FIT for a low-power MOSFET, 500 FIT for a medium-power device, and 5000 FIT for a power module without its driver (1 FIT $= 10^{-9}/h$). For standard power modules, a base failure rate of 100 FIT is commonly employed (Tu; Yang; Wang, 2019).

Furthermore, π_T is the correction factor for T_j different from 100 °C, given by Arrhenius law (Richardeau; Pham, 2013):

$$\pi_T = e^{-2114\left(\frac{1}{T_j+273}-\frac{1}{298}\right)}, \tag{3.7}$$

Since the junction temperature profile of the device varies over time, T_j maximum is considered (Richardeau; Pham, 2013). π_s is the acceleration voltage breakdown for the drain–source voltage by the empirical relation:

$$\pi_S = 0.045 e^{3.1 V_{sf}}, \tag{3.8}$$

where V_{sf} is the voltage stress factor.

Finally, π_E and π_A are described according to the type of application:

$$\pi_E = \begin{cases} 1 & \textit{Ground benign} \\ 7 & \textit{Naval sheltered} \\ 10 & \textit{Ground fixed} \\ 15 & \textit{Naval unsheltered} \\ 20 & \textit{Ground mobile}, \end{cases} \tag{3.9}$$

$$\pi_A = \begin{cases} 0.7 & \textit{Switching mode} \\ 1.5 & \textit{Linear mode}. \end{cases} \tag{3.10}$$

3.3 Wear-out Failure Region

The traditional reliability analysis of power electronic converters is based on empirical failure analysis related with historical data. Recently, the reliability engineering is going to the physics-of-failure approach (POF). POF analysis is based on the mission

profiles, type of failure mechanism and the related statistical model. Each mission profile leads to different stress distribution and each failure mechanism has different strength rates related to these profiles. Therefore, the power modules failure rate is strongly dependent on the mission profile and the type of wear-out fatigue. Considering the POF analysis, the failure rate evolution in the wear-out region can be modeled as illustrated in Fig. 22 and explained next.

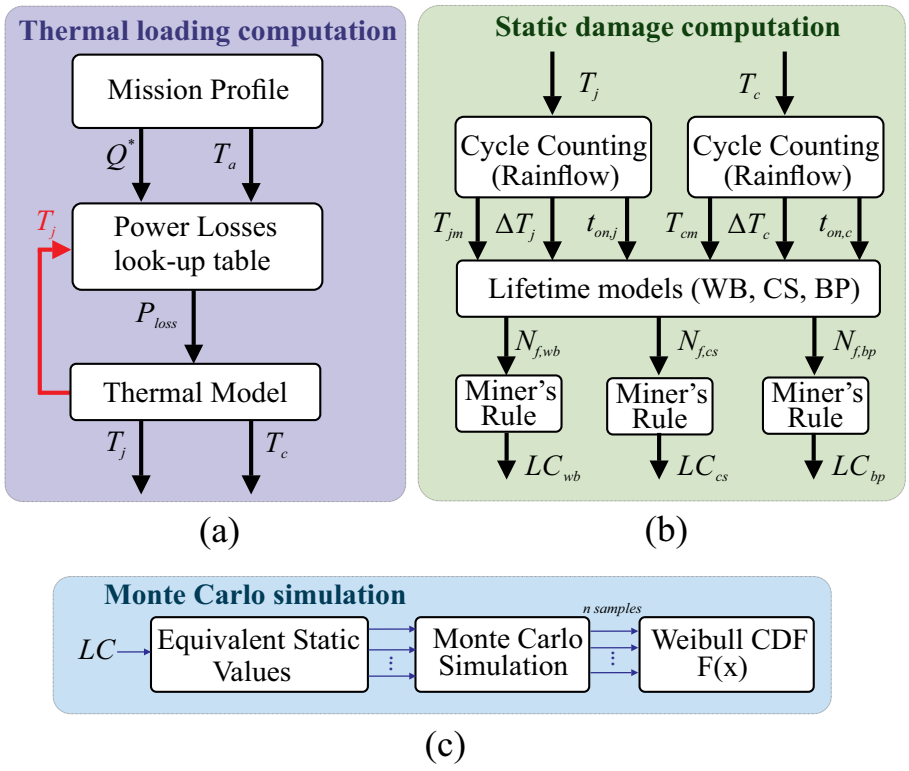

Figure 22 – Wear-out analysis flowchart: (a) Translation of the mission profile into thermal stresses; (b) Static damage computation through reliability model; (c) Monte Carlo simulation for computation of component and system-level reliability.

3.3.1 Thermal Loading Computation

Initially, the mission profiles are defined. Measurements of reactive power (Q^*) and ambient temperature (T_a) mission profiles are employed to define the system operating condition.

The conduction, switching losses and thermal impedances of the power modules are obtained from look-up tables created in PLECS environment based on the datasheets. Figure 23 shows the typical on-state characteristics and switching energies of the power modules extracted from the datasheets.

As observed, the power losses on temperature dependence is considered. Linear interpolation and extrapolation are used. Moreover, the switching energies are assumed proportional to the blocking voltage. One limitation of this approach is the influence of

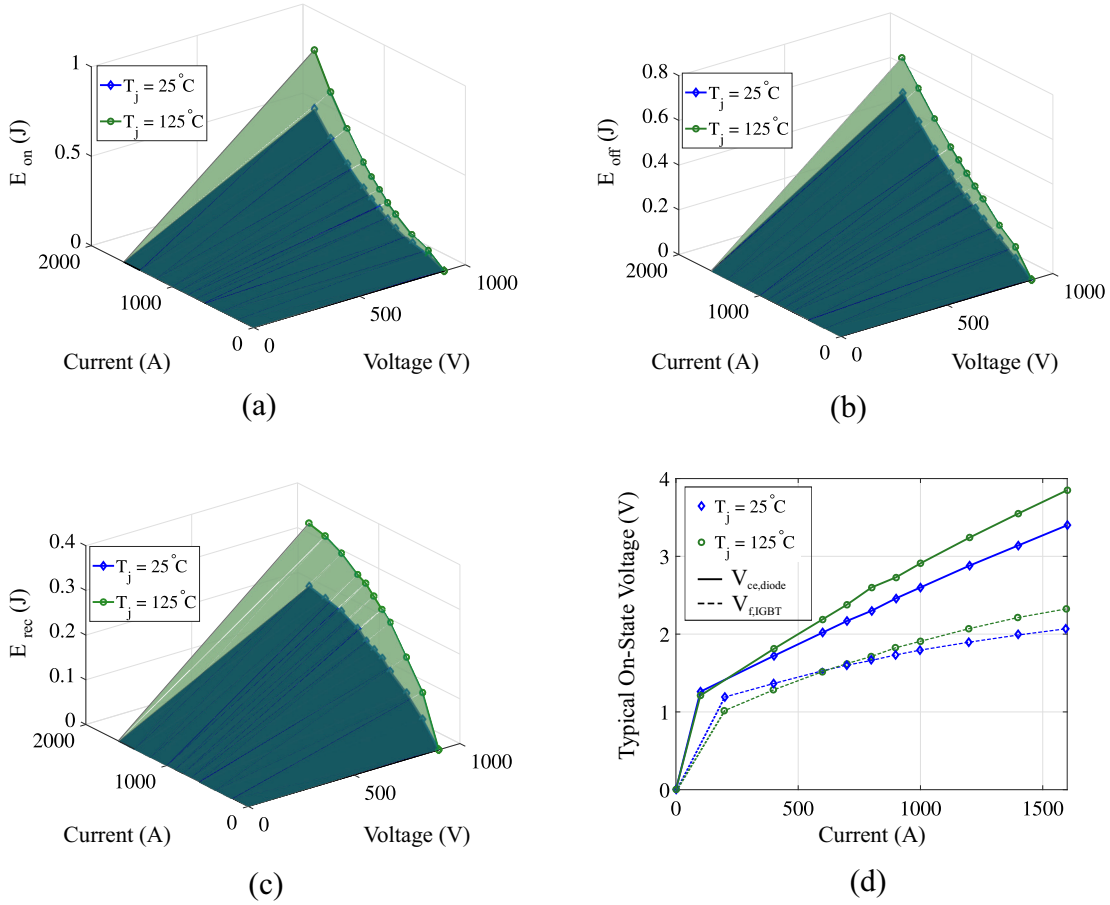

Figure 23 – Data extracted from a power module datasheet: (a) Turn-on switching energy (IGBT); (b) Turn-off switching energy (IGBT); (c) Reverse recovery energy (diode); (d) Typical IGBT on-state characteristics and diode forward characteristics. In this example, the part number 5SND 0800M170100 is considered.

converter layout (due to stray inductance) in switching losses, which is neglected (Sousa et al., 2017). Data from experimental characterization could be employed to deal with this issue. Nevertheless, this approach is time consuming and costly. Alternatively, this work considers power modules from the same manufacturer tested in similar conditions.

The hybrid thermal model proposed by (Ma et al., 2016) is employed to estimate the junction (T_j) and case temperature (T_c) of each power device, as observed in Fig. 24. The junction-to-case thermal impedance Z_{j-c} combines Cauer and Foster thermal networks to provide the best features of both models (Tu; Xu, 2011). The case-to-heatsink impedance Z_{c-h} is represented by a thermal resistance.

The heatsink-to-fluid impedance Z_{h-f} presents a parallel connection of the thermal resistance R_{h-f} and the capacitance C_{h-f}. The detailed view of the power module and water cooling plate is presented in Fig. 25 (a). A simplified heatsink model for power converter is illustrated in Fig. 25 (b). Heatsink parameters can be estimated through the simplified methodology proposed by Asimakopoulos et al. (2015). This methodology

considers an uniform temperature profile throughout the power devices baseplate solder and cooling plate. The heatsink geometry has a simple rectangular cross-section and is approximated by a simple orthogonal brick. Under such conditions, the heatsink parameters can be computed by:

$$R_{h-f} = \frac{d_h}{\kappa_h A_h}, \tag{3.11}$$

$$C_{h-f} = c_h \rho_h d_h A_h, \tag{3.12}$$

where d_h is the heatsink thickness, κ_h is the thermal conductivity of the heatsink material, A_h is the heatsink surface area, c_h is the specific heat capacity and ρ_h is the material density.

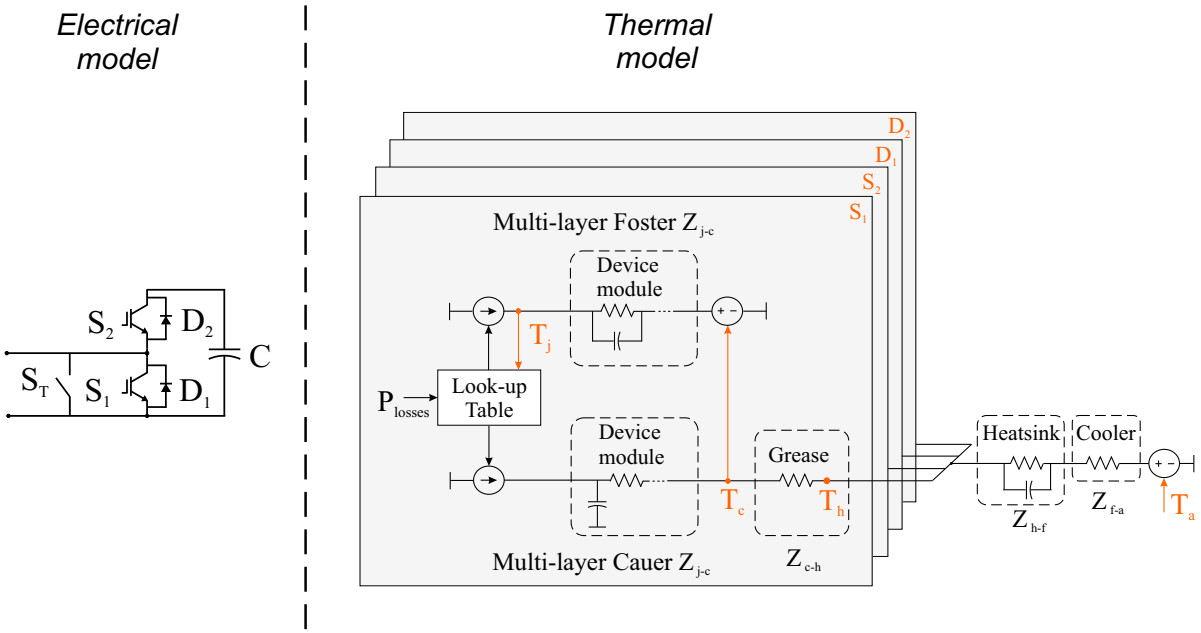

Figure 24 – Hybrid thermal model based on Foster and Cauer models with heatsink and cooling system.

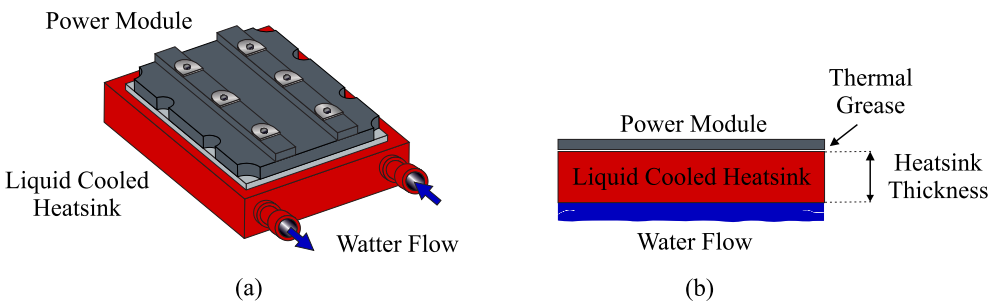

Figure 25 – Heatsink scheme of the water cooling system: (a) Detailed view; (b) Simplified model. Adapted from (Júnior et al., 2019).

The cooling system improves the heat exchange from the heatsink to the ambient, described by Z_{f-a}. This thermal resistance presents a series connection to the heatsink and can be calculated by (Asimakopoulos et al., 2015):

$$R_{f-a} = \frac{1}{f_{fc} A_h}, \tag{3.13}$$

where f_{fc} is the fluid flow convection coefficient (Incropera; DeWitt, 1996).

3.3.2 Static damage computation

The thermal cycling causes cyclic thermo-mechanical stresses in all joints and components of the power modules, which leads to wear-out failure in the device. Since the lifetime consumption (LC) evaluation is reached by the regular series of temperature profiles with constant average value, a rainflow counting method is employed (Liu et al., 2016) to provide the average temperature $T_{(j,c)m}$, cycle amplitude $\Delta T_{(j,c)}$ and heating time $t_{on,(j,c)}$. Thereby, the LC is obtained by using the Palmgren-Miner rule (Palmgren, 1924; Miner, 1945; Zeng et al., 2019):

$$LC = \sum_i \frac{n_i}{N_{f,i}}, \tag{3.14}$$

where n_i is the number of cycles obtained from rainflow algorithm and $N_{f,i}$ is the number of cycles to wear-out failure obtained for the i th stress condition. In this work, $N_{f,i}$ is evaluated through the ABB Hipak IGBT power module lifetime model (ABB, 2014). In general, the IGBT power module presents various materials with different thermal expansion coefficients. Therefore, the thermal cycling results in mechanical stress in all components and joints. Indeed, the most reported failure mechanisms in power modules are the baseplate solder fatigue, chip solder fatigue and bondwire lift-off. Figure 26 shows the ABB data for B_{10} lifetime (10% failure rate) for all critical joints (baseplate solder, chip solder and bondwire) (ABB, 2014).

As observed, only baseplate and chip solders are dependent on heating time. Moreover, higher $T_{(j,c)m}$, $\Delta T_{(j,c)}$ and $t_{on,(j,c)}$ values, reduce the B_{10} lifetime. Nevertheless, these curves are only suitable for thermal cycling values that fit in the data presented. Therefore, a data extrapolation approach is often used in the literature (Wagner; Khanh, 2014). In this work, a clip extrapolation in look-up tables is employed. This method returns the table data corresponding to the end of the breakpoint data set range. Finally, the lifetime model returns the number of cycles to failure N_f of the bondwire , chip solder and baseplate solder for each diode and IGBT of the modules.

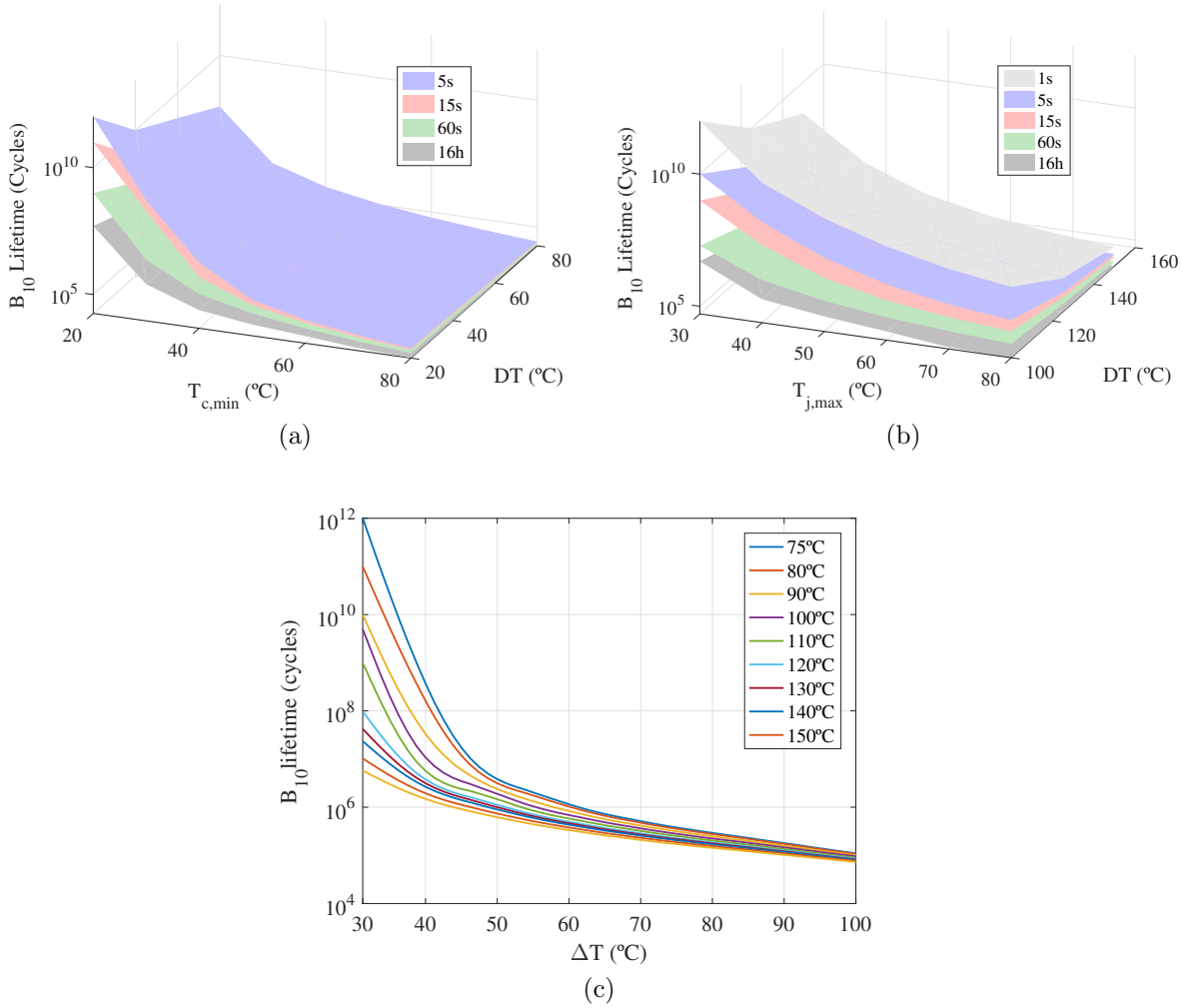

Figure 26 – B_{10} lifetime curves of Hipak IGBT module: (a) Baseplate solder; (b) Chip solder ; (c) Bondwire

3.3.3 Monte Carlo Simulation

Since the power devices present parametric variations due to the manufacturing process and stress variation (Sangwongwanich et al., 2018), the lifetime is usually expressed in terms of probabilities. Therefore, the dynamic values $T_{(j,c)m}$, $\Delta T_{(j,c)}$ and $t_{on,(j,c)}$ obtained by rainflow algorithm are transformed into equivalent static values, $T'_{(j,c)m}$, $\Delta T'_{(j,c)}$ and $t'_{on,(j,c)}$ using the methodology proposed by (Reigosa et al., 2016). The static value is a power cycling with constant parameters (amplitude, average value and heating time) which provides the same LC computed by Eq. (3.14). Therefore, a statistical analysis based on Monte Carlo simulation is employed (Reigosa et al., 2016).

Once the equivalent static values have been obtained, a variation of 5% is applied in these parameters and in the lifetime model used. A normal distribution with standard deviation σ and the mean value μ is adopted. A confidence interval of 99.73% is chosen, as illustrated in Fig. 27. Then, the Monte Carlo simulation is performed with $10,000$ samples. The lifetime distribution obtained from Monte Carlo simulation is fitted with the Weibull

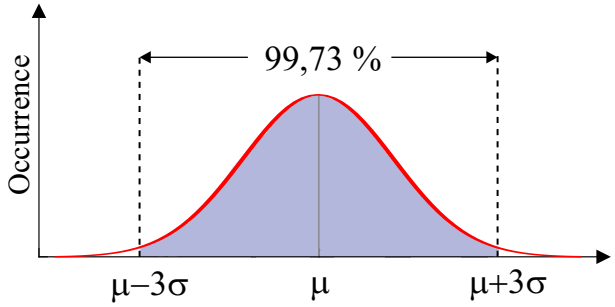

Figure 27 – Normal distribution showing how 5% was considered in all parameters (lifetime model and its inputs)

PDF $f(x)$ (Sangwongwanich et al., 2018), given by:

$$f(x) = \frac{\beta}{\eta^{\beta}} x^{(\beta-1)} exp\left[-\left(\frac{x}{\eta}\right)^{\beta}\right], \tag{3.15}$$

where β is the shape parameter, η is the scale parameter, and x is the operation time. The cumulative density function (CDF), also called unreliability function $F(x)$, represents the proportion of population failure, according to the time obtained through the integral of PDF, given as:

$$F(x) = \int_0^x f(x)dx, \tag{3.16}$$

Since IGBT and diode are distinctly analyzed for wear-out failure, the reliability function for each component can be calculated as:

$$R_{Comp,wf}(x) = 1 - F_{Comp,wf}(x), \tag{3.17}$$

3.4 System-Level Reliability

The system-level reliability block diagram of MMCC is subdivided into three hierarchical levels: MMCC-level, arm-level and cell-level, as observed in Fig. 28. In each hierarchical level, the reliability block diagram is used to represent the reliability relationship of MMCC components. All six arms and auxiliary device are required in good state for the MMCC normal operation. Hence, they are connected in series from reliability point of view. In this section, only k non-redundant cells are considered.

3.4.1 Cell-Level Reliability

Cell-level reliability can be evaluated as a combination of component reliability considering different mechanisms of failure. Although MMCC cells are composed of more

components, such as capacitors and gate drivers, the reliability analysis will be performed considering only the two IGBT power modules (IGBT with anti-parallel diode). The cell can operate normally only if all components are working properly.

Therefore, the cell-level reliability function for constant failure region is given by:

$$R_{cell,cf}(x) = R_{IGBT_1,cf}(x)R_{IGBT_2,cf}(x), \tag{3.18}$$

where $R_{IGBT_1,cf}$ and $R_{IGBT_2,cf}$ are the reliability functions of the lower and upper IGBT power module of each cell, respectively. Since the same failure rate is assumed for both IGBT power modules in one converter cell, Eq. (3.18) can be reformulated as (Tu; Yang; Wang, 2019):

$$R_{cell,cf}(x) = e^{-\lambda_{cell}x}, \tag{3.19}$$

where λ_{cell} is the constant cell failure rate which is $2\lambda_{IGBT}$.

The cell-level reliability function for wear-out failure region is calculated as:

$$R_{cell,wf}(x) = \prod_{i=1}^{4} R_{Comp(i),wf}(x), \tag{3.20}$$

where i indicates each discrete semiconductor device (i.e., S_1, S_2, D_1 and D_2) for each cell.

The complete cell-level reliability can be realized through the product of constant and wear-out cell-reliability functions (Scheuermann; Junghaenel, 2018), as follows:

$$R_{cell}(x) = R_{cell,cf}(x)R_{cell,wf}(x). \tag{3.21}$$

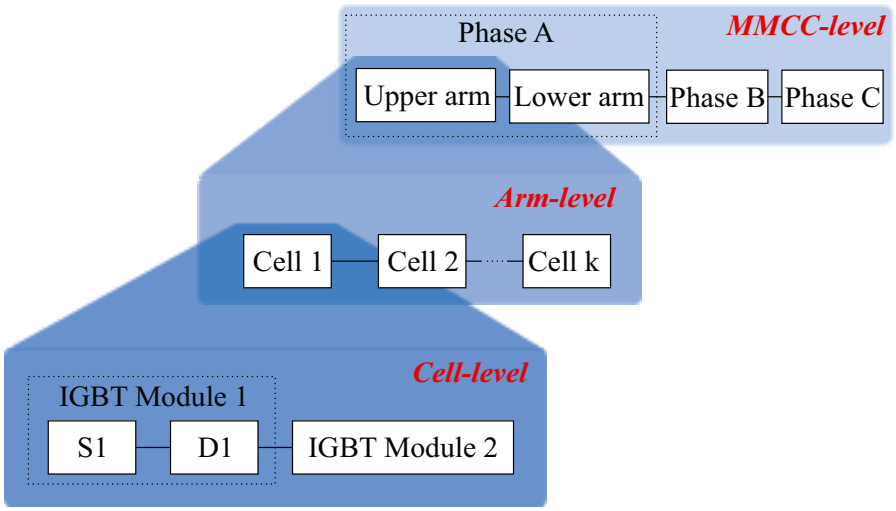

Figure 28 – System-level reliability block diagram of MMCC.

3.4.2 Arm-Level Reliability

Since the converter operates only with non-redundant cells, the arm-level reliability is the product of the reliability functions of k non-redundant cells. Assuming that each cell is independent and identical, the arm-level reliability function can be evaluated as follows (Wang et al., 2017):

$$R_{arm}(x) = \prod_{l=1}^{k} R_{cell(l)}(x). \tag{3.22}$$

3.4.3 MMCC-Level Reliability

As observed in Fig. 9, the three-phase MMCC presents six arms in the structure. Assuming that each arm is independent and identical, the MMCC system-level reliability can be evaluated by:

$$R_{MMCC}(x) = \prod_{l=1}^{6} R_{arm}(x). \tag{3.23}$$

3.5 Case Study

A 17 MVA MMCC-STATCOM with line-to-line voltage of 13.8 kV at the point of common coupling (PCC) is considered. Based on the topology presented in Fig. 9, the simulations were performed using the PLECS and MATLAB software systems. PLECS simulations are used to estimate the MMCC energy losses and the lifetime evaluation is obtained by MATLAB software.

The converter is submitted to a mission profile based on a reactive power demand and ambient temperature measurements in southeastern Brazil, as presented in Fig. 29.

Table 8 shows the part numbers employed in the MMCC designs. Four different ABB HiPak IGBTs modules with blocking voltage capability range between 1.7 kV and 6.5 kV are considered. Commercially available modules with rated current close to 800 A are selected. The designs of each DSCC-MMCC-based STATCOM are obtained by the methodology presented in section 2.2. Therefore, the main circuit parameters are presented in Tab. 5.

Table 8 – HiPak IGBT modules specifications for four proposed solutions.

Voltage (V)	**Current (A)**	**Part Number**	**Case**
1700	800	5SND 0800M170100	C_{17}
3300	800	5SNA 0800N330100	C_{33}
4500	800	5SNA 0800J450300	C_{45}
6500	750	5SNA 0750G650300	C_{65}

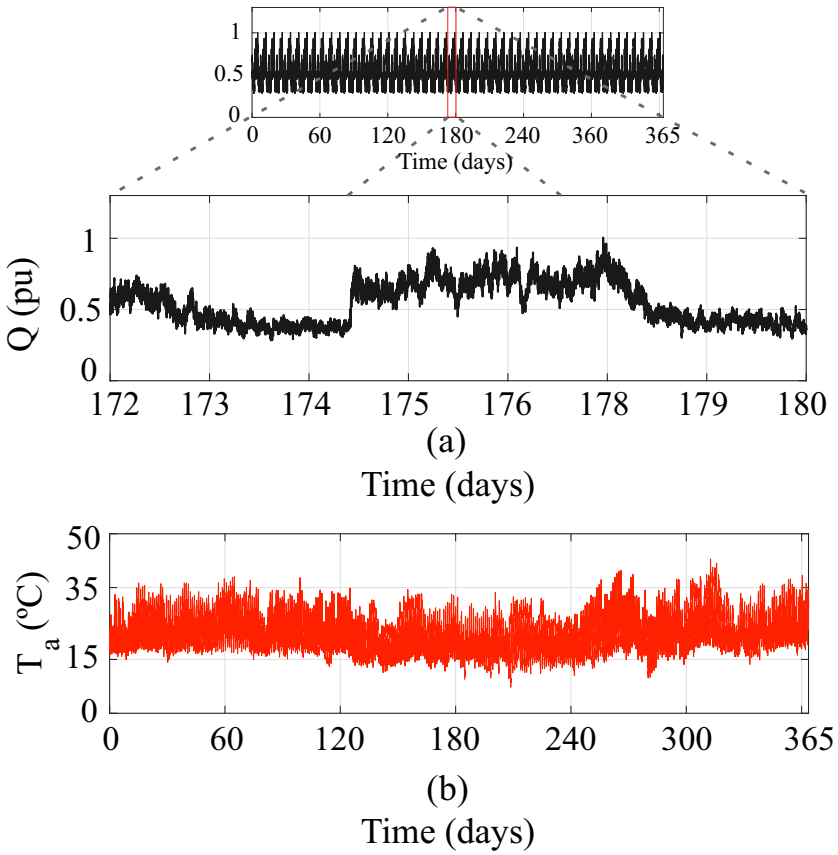

Figure 29 – Mission profiles with a sampling time of 5 min: (a) Reactive Power; (b) Ambient Temperature.

Figure 30 presents the typical HiPak power devices curves extracted from datasheets. All curves are evaluated for a junction temperature of 25 °C. The IGBT and diode conduction power losses can be evaluation through the curves shown in Fig. 30 (a) and (b). Moreover, Figure 30 (c) and (d) illustrated the IGBT and diode switching losses. All utilization factors have similar values. The IGBT switching energy curves include both turn-on and turn-off switching energies data.

The data used in the power losses and thermal impedances Z_{j-c} and Z_{c-h} are extracted from the datasheets. Figure 31 presents the normalized transient thermal impedances for semiconductor devices. Moreover, Table 9 presents the Cauer parameters of the junction-to-case thermal impedance based in the Foster parameters. The Foster parameters extracted from datasheets were converted to Cauer parameters through software PLECS.

Regarding heatsink parameters, the values of R_{h-f} and C_{h-f} vary according to the heatsink area and thickness. In this work, the area is considered to be equal to the total area of the power module obtained from the device datasheet. Furthermore, aluminum heatsinks with 3 cm of thickness are employed (Asimakopoulos et al., 2015).

The water-cooling system are evaluated to ensure similar temperature stresses in

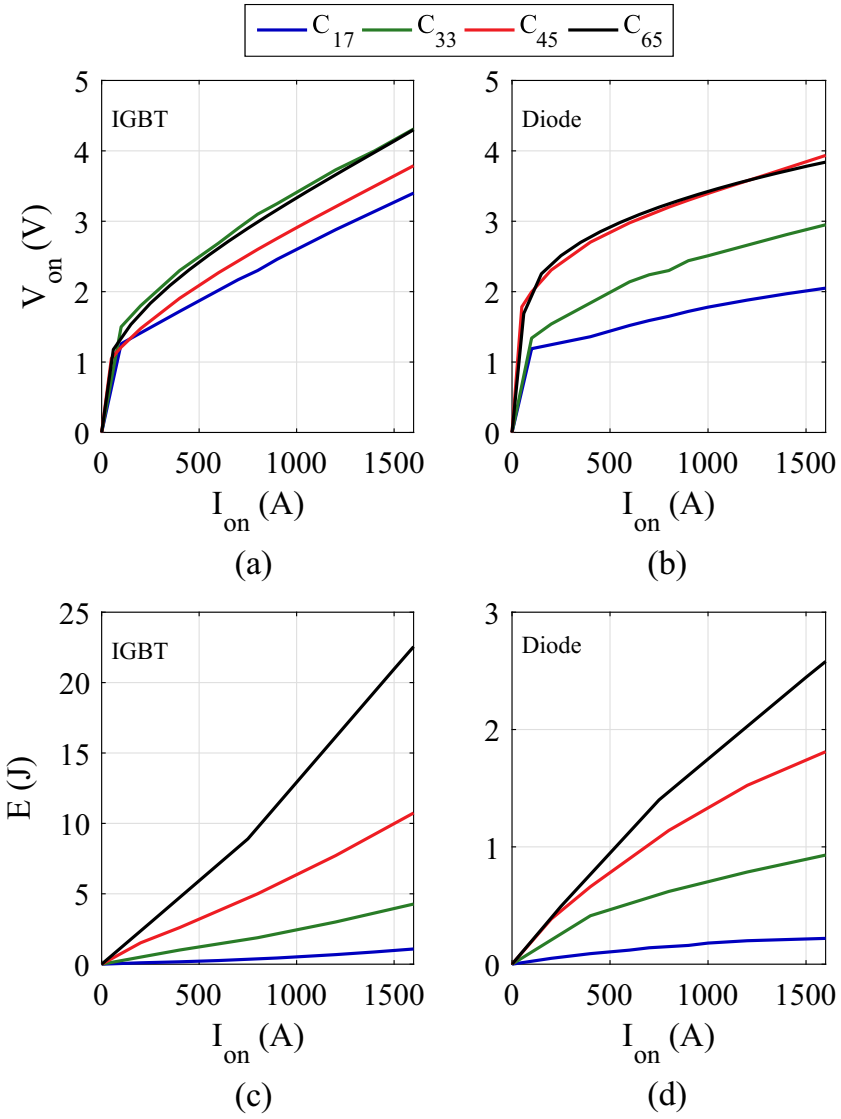

Figure 30 – Typical power devices curves extracted from datasheets: (a) IGBT on-state characteristics; (b) Diode forward characteristics; (c) IGBT switching energies per pulse; (d) Diode reverse recovery characteristics.

each IGBTs module solution (Incropera; DeWitt, 1996; Farias et al., 2018). The water flow convection coefficient f_{fc} can range from 50 to 2500 $W/(m^2K)$, depending on the speed and type of water flow, temperature dependent properties, and pressure (Júnior et al., 2019). The manufacturer indicates maximum values of $T_{j,max} = 150$ °C and $T_{c,max} = 125$ °C.

The typical lifetime target of power electronics systems, from industry perspective, is described in (Falck et al., 2018). For STATCOM applications, such as industrial and wind power systems, it is reported an expected lifetime of around 20 years (Falck et al., 2018; Wang et al., 2014). Thereby, the MMCC lifetime target is defined as $x_0 = 20$ years of operation.

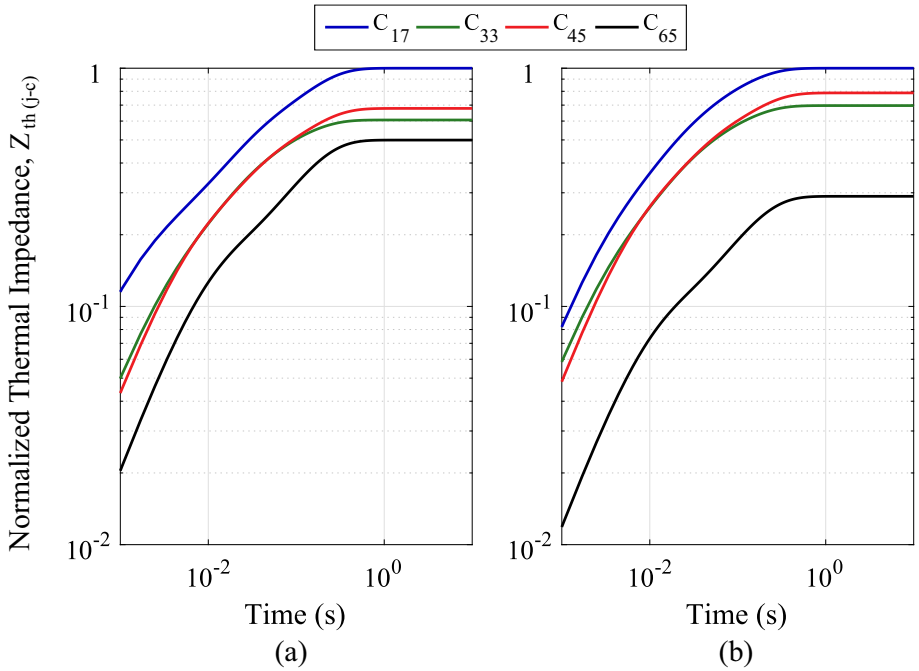

Figure 31 – Normalized transient thermal impedance characteristics for all cases: (a) IGBT; (b) Diode.

Table 9 – Cauer parameters of the junction-to-case and case-to-heatsink thermal impedances.

Case	Device	Parameter	$\mathbf{Z}_{j-c}$				$\mathbf{R}_{c-h}$ (K/W)
C_{17}	IGBT	R_i (K/W)	0.0018	0.0018	0.0060	0.0110	0.024
		C_i (J/K)	0.4162	1.1210	3.2270	12.170	-
	Diode	R_i (K/W)	0.0047	0.0067	0.0096	0.0150	0.048
		C_i (J/K)	0.4240	1.482	2.883	7.5910	-
C_{33}	IGBT	R_i (K/W)	0.0017	0.0025	0.0034	0.0050	0.012
		C_i (J/K)	1.1878	4.3056	8.5513	22.137	-
	Diode	R_i (K/W)	0.0035	0.0050	0.0068	0.0098	0.024
		C_i (J/K)	0.5865	2.1251	4.2084	11.453	-
C_{45}	IGBT	R_i (K/W)	0.0028	0.0045	0.0070	-	0.013
		C_i (J/K)	1.3159	4.9157	20.361	-	-
	Diode	R_i (K/W)	0.0059	0.0093	0.0134	-	0.027
		C_i (J/K)	0.6986	2.5225	10.487	-	-
C_{45}	IGBT	R_i (K/W)	0.0027	0.0078	-	-	0.009
		C_i (J/K)	2.5078	16.720	-	-	-
	Diode	R_i (K/W)	0.0057	0.0155	-	-	0.018
		C_i (J/K)	1.1926	8.0103	-	-	-

3.5.1 Results

Initially, semiconductors power losses for all cases are shown in Fig. 32. All cases are evaluated for a junction temperature of 25 °C and 1.0 pu of reactive power in inductive operation. As observed, an increase in the blocking voltages of power devices causes an increase in switching losses. This result is consistent with the curves extracted from

datasheets shown in Fig. 30. Furthermore, diodes with higher blocking voltages present higher conduction losses, whereas this relationship is not straightforward for IGBTs. The IGBTs based on C_{33} solution present higher conduction losses. Moreover, the design based on C_{17} has the lowest total power losses in a cell.

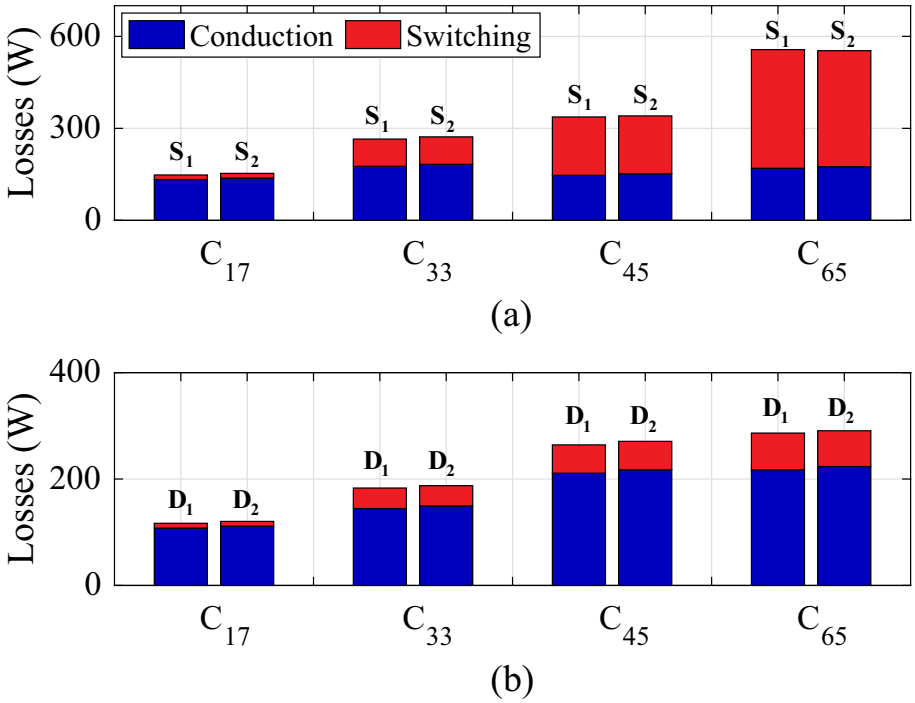

Figure 32 – Power losses for all cases of power devices: (a) S_1 and S_2; (b) D_1 and D_2.

The power losses, including conduction and switching losses, of a power semiconductor device are obtained. Fig. 33 shows the power losses for different operating conditions. For simplification, only the losses in the IGBT S_1 are shown. As observed, an increase in rated power or junction temperature in the power devices, cause an increase in power losses. Moreover, power modules with higher blocking voltages present higher power losses.

The water flow convection coefficient is adjusted to maintain the average heatsink temperature close to 60 °C, for all cases. Table 10 presents the parameters of the heatsinks and cooling system. As observed, the resistance and capacitance parameters of the heatsink have approximate values due to the similar dimensions of the power modules. Therefore, a lower thermal resistance in the cooling system is required for the power modules that present higher losses.

Table 10 – Heatsink and cooling system parameters.

Case	$\mathbf{R}_{h-f}$ **(K/W)**	$\mathbf{C}_{h-f}$ **(J/K)**	$\mathbf{R}_{f-a}$ **(K/W)**
C_{17}	0.007	1327	0.130
C_{33}	0.007	1327	0.070
C_{45}	0.007	1327	0.050
C_{65}	0.005	1939	0.030

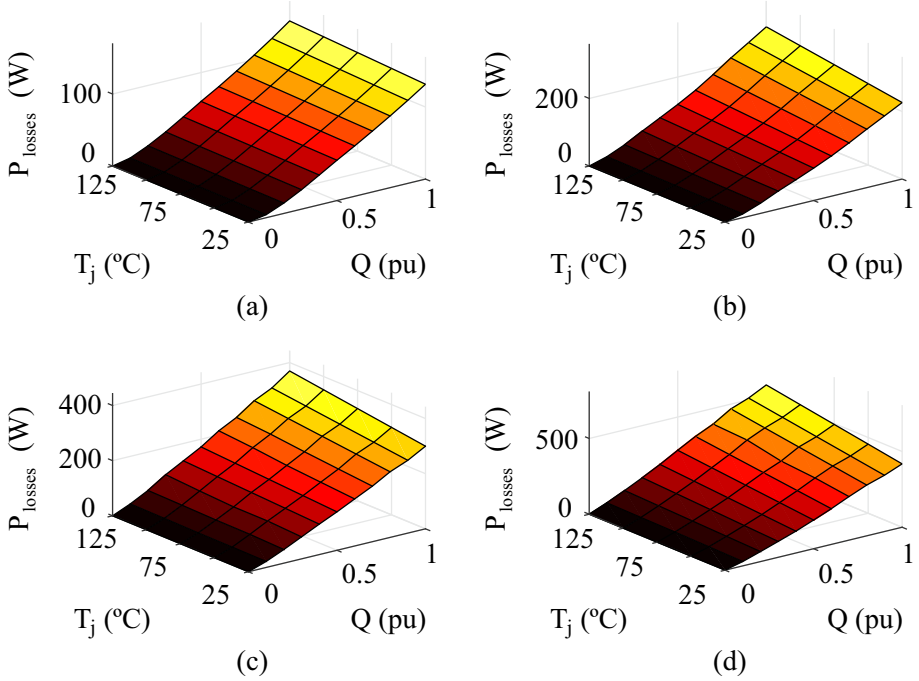

Figure 33 – Power losses of IGBT S_1 for the cases: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

Based on the application mission profile, the diode D_2 is the most stressed device in a cell. Figure 34 presents the junction and case temperature in D_2 for all solutions. As observed, the maximum junction and case temperature are approximately 120 °C and 110 °C, respectively. All cases have similar thermal stresses.

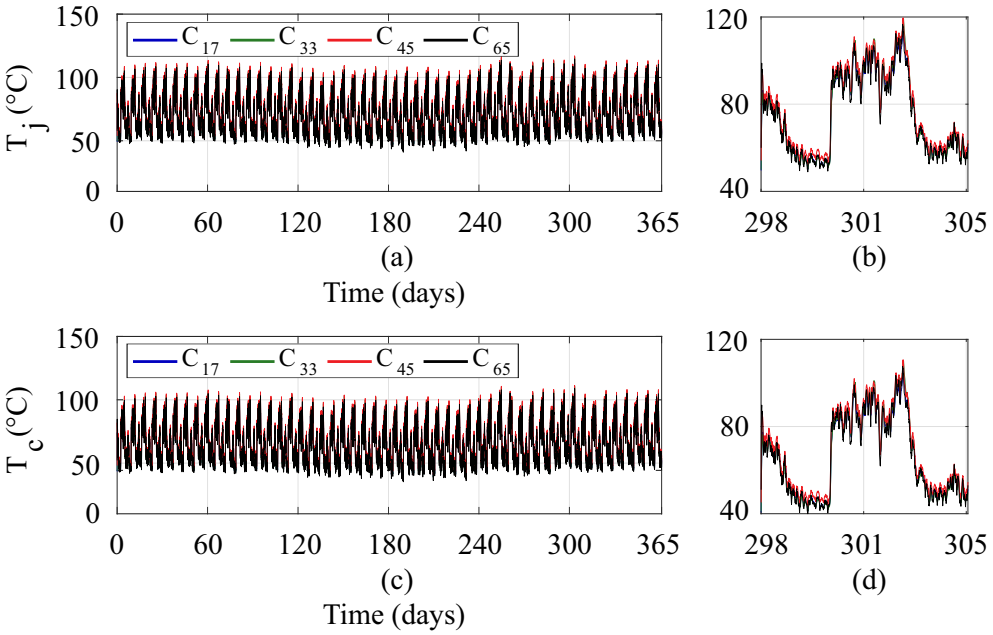

Figure 34 – Temperatures of the more stressed device D_2 in a cell for four designs: (a) Junction temperature; (b) Detailed view of (a); (c) Case temperature; (d) Detailed view of (c).

Considering the $T_{j,max} = 120$ °C, the IGBT failure rate is calculated by Eq. 3.6, as

shown in Tab. 11. C_{17} presents the lowest FIT among the solutions.

Table 11 – Parameters for evaluation of IGBT failure rate for different MMCC design.

Parameter	$\mathbf{C_{17}}$	$\mathbf{C_{33}}$	$\mathbf{C_{45}}$	$\mathbf{C_{65}}$
π_T	5.12	5.53	5.59	5.39
π_S	0.21	0.21	0.20	0.20
π_E	1.00	1.00	1.00	1.00
π_A	0.70	0.70	0.70	0.70
λ_{IGBT} (FIT)	75.26	81.29	78.26	75.46

Since the thermal cycling is obtained, the rainflow algorithm and the lifetime model are applied. Table 12 presents the static LC in one year for the critical joints of the power devices based on C_{17} solution. The baseplate solder is the most damaged region. Therefore, in the Monte Carlo simulation, the wear-out failure in the baseplate solder is analyzed (Sousa et al., 2018).

Table 12 – Static LC of devices by different joints based on C_{17} solution.

Devices	**Wirebond**	**Chip solder**	**Baseplate solder**
S_1	$0.05 \cdot 10^{-3}$	$1.03 \cdot 10^{-3}$	$3.95 \cdot 10^{-3}$
S_2	$0.06 \cdot 10^{-3}$	$1.05 \cdot 10^{-3}$	$4.01 \cdot 10^{-3}$
D_1	$0.06 \cdot 10^{-3}$	$1.14 \cdot 10^{-3}$	$4.16 \cdot 10^{-3}$
D_2	$0.07 \cdot 10^{-3}$	$1.15 \cdot 10^{-3}$	$4.20 \cdot 10^{-3}$

The Weibull PDF is obtained by employing the static values and the lifetime model into the Monte Carlo simulation with $10,000$ samples and 5% variation. For the sake of simplicity, only the lifetime distribution of D_2 device is presented. Figure 35 shows the result obtained for the four cases. Figure 35 (c) and (d) show that the 4.5 kV and 6.5 kV voltage classes have more concentrated distribution due to higher thermal losses and stresses in the devices.

The previously lifetime analysis is based on component-level assessment. A system-level reliability model presented in section 3.4 is used to obtain a converter-level reliability assessment. Figure 36 presents both wear-out and constant failure rates contributions on the MMCC system-level reliability. The contribution of each failure rate in the system reliability is derived from Eq. (3.21). As observed, the most significant contribution in the MMCC reliability is given by the constant failure rate in the initial years. Moreover, the random failures have more influence on the converter lifetime for designs with more cells.

The MMCC system-level reliability for the four analyzed cases are shown in Fig. 37. As observed, solutions with the highest number of cells present smaller system-level reliability. The solution based on the design C_{65} presents the highest reliability, 25.97% for 20 years of operation. Furthermore, C_{17} has the lowest reliability, 0.67%.

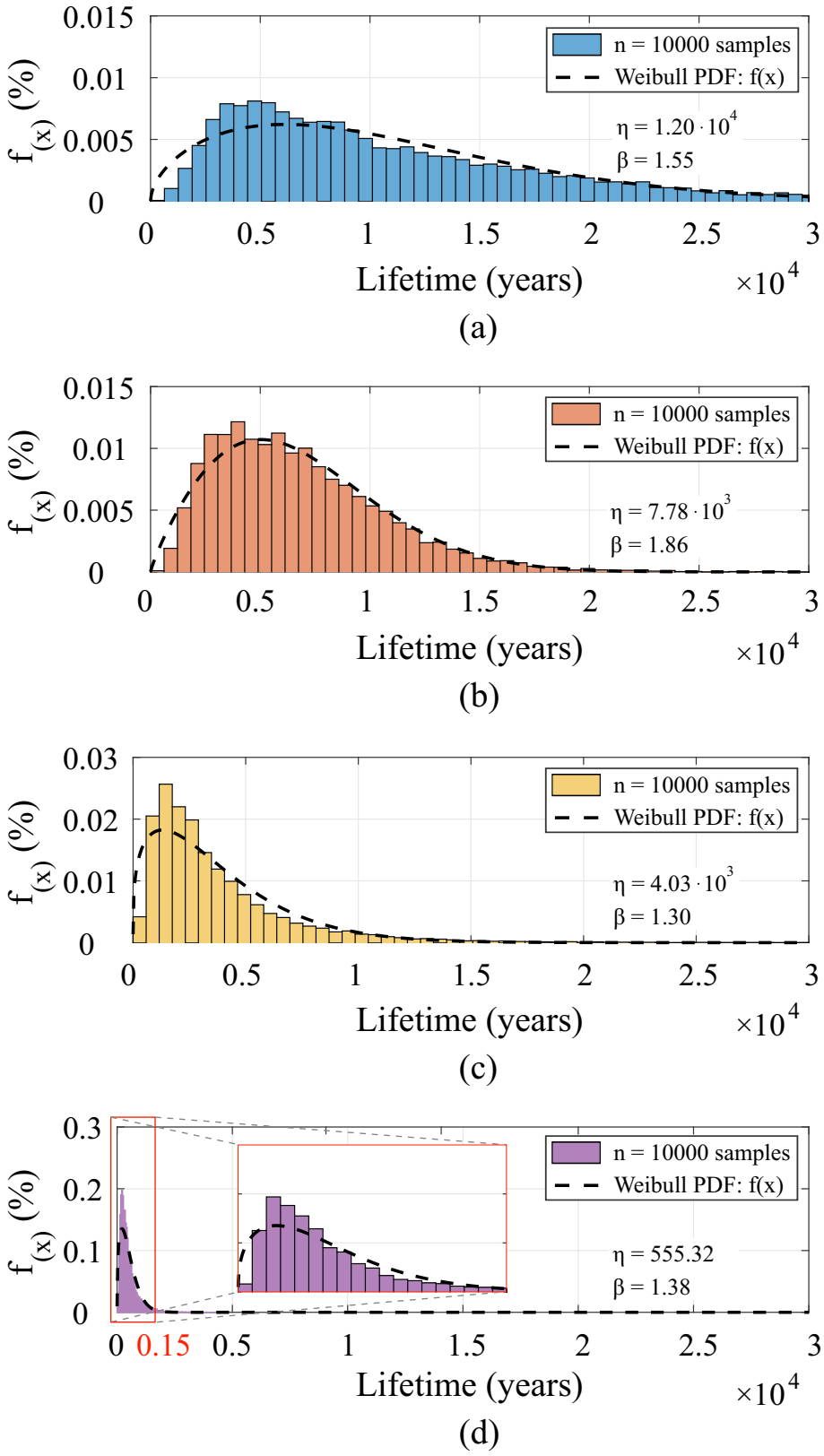

Figure 35 – Lifetime distribution (i.e., the Weibull PDF function) of the most stressed device D_2 for cases: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

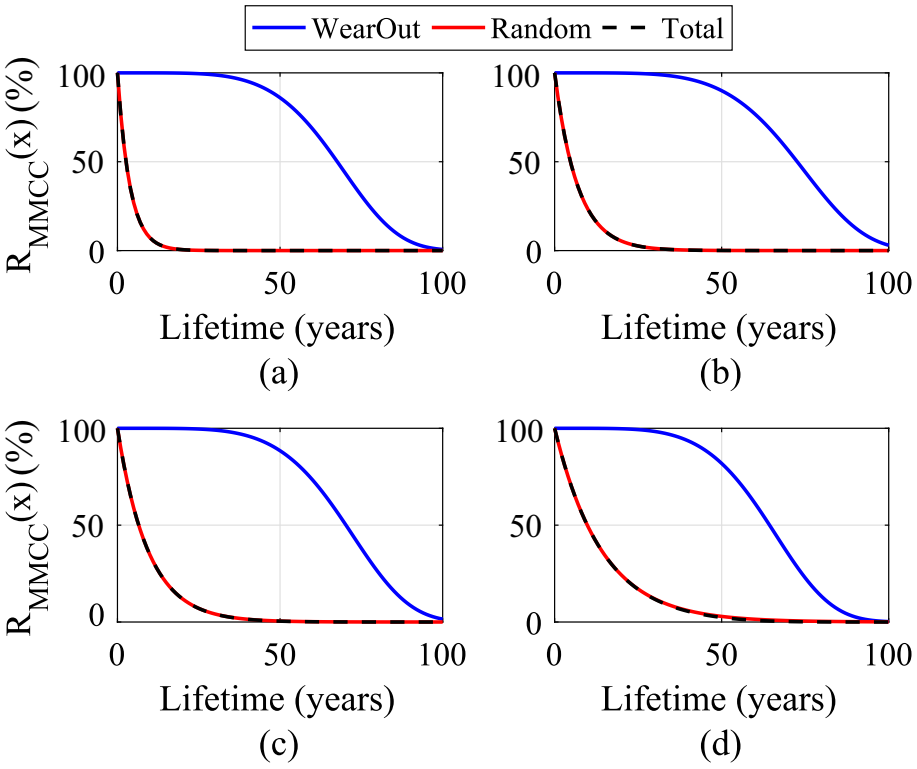

Figure 36 – MMCC system-level reliability-based on wear-out and constant failure rates contributions factors and the total converter reliability: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

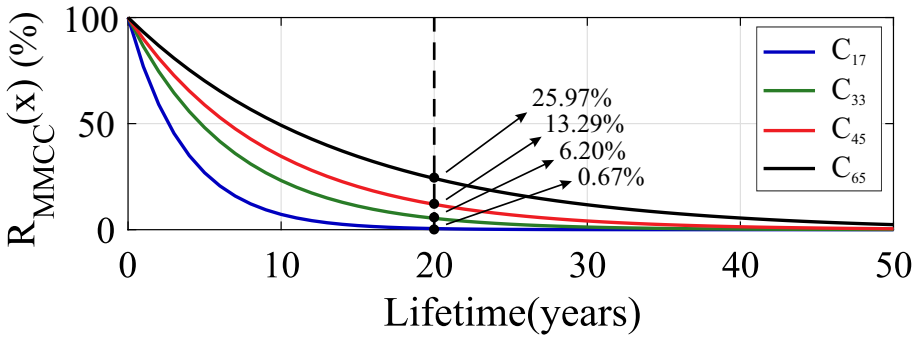

Figure 37 – MMCC system-level reliability function for different solutions.

3.6 Chapter Conclusions

This chapter proposed a combined reliability-oriented design for DSCC-MMCC-based STATCOM. Both random and wear-out failures are considered in the model. As observed, random cell failures are dominant in the converter. Nevertheless, wear-out failure has an influence on the converter reliability close to the end-of-life period. Four different realizations of the DSCC-MMCC-based STATCOM were compared. Solution based on the design C_{65} presents the highest reliability, 25.97% for 20 years of converter operation.

Futhermore, the reliability-level requirements can be stricter depending on the applied B_x lifetime approach. Considering B_{10} lifetime, all solutions present reliability

below the defined target. To improve the reliability, the wear-out failures can be predicted (to some extent) and even avoided at the design stage. However, the lifetime of the converter is mainly limited by the effect of random failures, in this case study. Under such conditions, to overcome these events, redundant cells shall be added during the converter design. The next chapter discusses redundancy strategies and proposes a reliability-oriented design method based on redundancy factor selection.

4 Redundancy Design Based on Reliability Assessment

MMCC family is often featured with its robustness in terms of cell failures. When failures are identified, the corresponding cell should be bypassed (Son et al., 2012). Under such conditions, some redundancy strategy must be used to ensure the converter remains operating without affecting the overall performance (Davies et al., 2017; Tu; Yang; Wang, 2019). Usually, this condition is fulfilled for a perceptual number of cell failures (Xu; Zhao; Zhao, 2016). This perceptual number of failures is commonly known as *redundancy factor* (f_r). An empirical redundancy factor of 10% is proposed in (Ahmed et al., 2015). This means that the converter operation can operate if less than 10% of the cells fail. On the other hand, some works propose the evaluation of the redundancy factor based on the failure rate of the devices (Xu; Jing; Zhao, 2018; Tu; Yang; Wang, 2019; Wang et al., 2017).

Xu, Jing and Zhao (2018) proposes an algorithm to evaluate the number of redundant cells required based on numerical solutions. The results show that installing of redundant cells can significantly improve the MMCC arm-reliability if the design considers cells correlations. Another numerical solution is presented by Tu, Yang and Wang (2019). According to a quantitative reliability analysis result, the redundant designs which meet the reliability requirement is identified. Wang et al. (2017) proposes a mathematical reliability model of MMCC considering periodic preventive maintenance. The results indicate that the MMCC cost can be reduced by properly analyzing the interaction between maintenance interval and the required redundancy levels.

Nevertheless, these works only consider the constant failure rate region of the bathtub curve. Therefore, this chapter aims to propose a methodology for redundancy factor selection considering both wear-out and constant failure.

4.1 Redundancy Strategies for DSCC-MMCC

Redundancy strategies can be implemented through additional cells m in the converter structure, as illustrated in Figure 9. In general, the redundant cells are usually operated in active mode or standby mode, as described by Chen, Yu and Li (2019):

- *active mode*: the redundant cells operate "actively". Essentially, no difference exists between the redundant cells and non-redundant cells. The arm continues to operate upon cell failures as long as the number of healthy cells is larger than k. The

active mode operates with or without load-sharing effect (Chen; Yu; Li, 2019). A load-sharing rule dictates how stress or load is redistributed to the surviving components after a component fails or degrades within the system.

- *standby mode*: the redundant cells are bypassed and initially discharged. When failures occur, the corresponding faulty cells are bypassed from the arm and redundant cells are inserted into the main circuit

Nevertheless, the redundancy of the MMCC can be implemented without any additional cells. The previous classifications are given according to the existence or not of redundant cell. Alternatively, the redundancy strategies can be classified into four strategies based on the terminology described by Farias et al. (2018): Redundancy based on Additional Cells (RAC), Optimized Redundancy based on Additional Cells (RACO), Redundancy based on Spare Cells (RSC) and Standard Redundancy operation (SR). The classification of the DSCC-MMCC redundancy strategies is illustrated in Fig. 38.

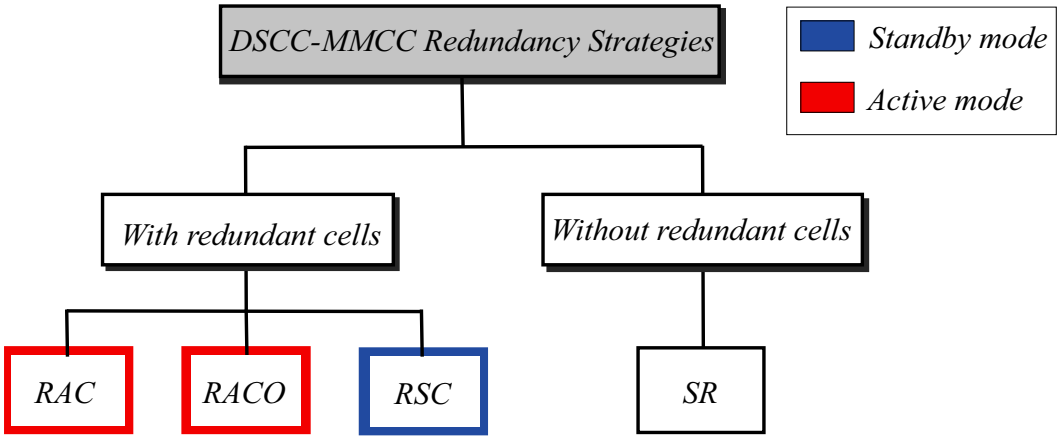

Figure 38 – Classification of the DSCC-MMCC redundancy strategies.

The RAC strategy operates the converter with more cells than the rated number. When failures occur, the faulty cells are bypassed and the control strategy will be dynamically adapted for the new number of cells (Saad et al., 2015). Two approaches are possible: in the first approach, all cell voltages are controlled at the rated reference value. The reference voltage does not need to be increased after failures. Therefore, less significant transients are observed. However, RAC leads to more switching losses in steady-state and can affect the overall efficiency (Ahmed et al., 2015). A second approach controls the cell voltage to a reduced value under normal conditions. In this case, the voltage stresses in power devices are reduced. Therefore, the switching losses are reduced, leading to an increase in the converter efficiency. This strategy is referred in this chapter to as optimized redundancy based on additional cells (RACO) (Farias et al., 2018).

The RSC is based on the spare cells concept (Son et al., 2012). Under normal conditions, the spare cells are always bypassed (Li et al., 2015). When failures occur,

the faulty cells are replaced by spare cells. The spare cell is then charged by the control strategy. It must be remarked that RSC does not change the number of operating cells. Therefore, no control adaptation is employed. However, if compared to the other strategies, RSC results in a larger transient unbalance in capacitor voltages, since the spare cells are discharged when it is inserted into the MMCC circuit.

Konstantinou, Ciobotaru and Agelidis (2012) and Ahmed et al. (2015) study the SR strategy. When failures occur, the voltage in the remaining operating cells is increased. The number of levels at the converter output is reduced while the overmodulation is avoided. According to Konstantinou, Ciobotaru and Agelidis (2012), since MMCC has been built with hundreds of cells, to reduce the output voltage levels would be an economic solution. Nevertheless, in practical applications, the safe operating area of the cells is generally 50 - 60% of the semiconductors blocking voltages (ABB, 2017). Therefore, the SR redundancy factor is limited by the maximum voltage stresses at the semiconductor devices and cell capacitors.

Farias et al. (2018) present the comparison of the redundancy strategies applied in DSCC-MMCC. Table 13 summarizes the main characteristics of the studied redundancy strategies (Farias et al., 2018). The qualitative terms excellent, good and regular indicate the best, average and worst performance, respectively.

Table 13 – Comparison of the redundancy strategies applied in DSCC-MMCC (Farias et al., 2018).

Parameter	**RAC**	**RACO**	**RSC**	**SR**
Cell voltage dynamics	Excellent	Good	Regular	Good
Output current dynamics	Excellent	Good	Regular	Good
Power losses	Regular	Good	Excellent	Excellent
Control complexity	Regular	Regular	Excellent	Good
CAPEX	Regular	Regular	Regular	Excellent

Although the previous comparison addressed several features of MMCC redundancy strategies, the converter reliability analysis is missing. Indeed, the system-level reliability in the random failure period is often modeled by statistical analysis, considering both active and standby redundancy strategies (Xu; Jing; Zhao, 2018). However, in wear-out failure period, only the reliability strategy based on active redundancy is discussed (Jia et al., 2017). Due to the complexity of the reliability modeling based on wear-out failures considering standby redundancy, only active redundant cells operating without load-sharing effect are taken into account in this work. Disregarding the load-sharing effect, the number of operating cells in a phase unit is always equal to k (Konstantinou et al., 2013), which means the number of operating cells in each arm during a fundamental period ranges from 0 to k. The reference voltage of each cell remains unchanged, and the output levels of the arm voltage is not influenced by a cell failure. The inclusion of redundant cells results in an increase of the number of cells that delivers zero voltage (i.e., in bypass mode).

4.2 System-level reliability-based redundancy design

The MMCC arm-level reliability function can be evaluated by Eq. (3.22), only when non-redundant cells are employed. However, when redundant cells are employed in DSCC-MMCC, the arm-level reliability block diagram is changed as illustrated in Fig. 39. As observed, active redundant cells are operating cells in terms of reliability block diagram (Tu; Yang; Wang, 2019). Fig. 39 (b) shows one failure of non-redundant cell. In this case, the system will continue to operate until the number of failures exceeds the number of redundant cells m. It is noteworthy that the failure can occur in a redundant cell, since there is no difference between the redundant cells and non-redundant cells structure. Under such conditions, the cell-level reliability can be evaluated according to the section 3.4.1.

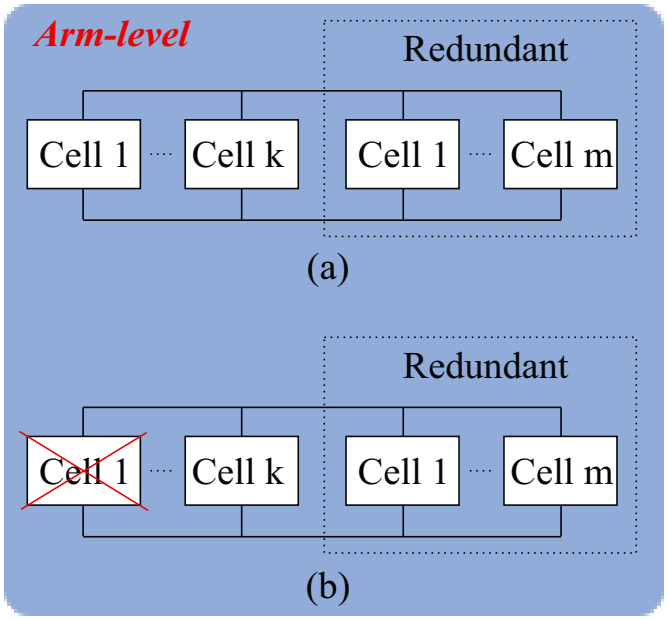

Figure 39 – Arm-level reliability block diagram of MMCC considering redundant cells: (a) without cell failure; (b) with one cell failure.

Since the active mode without load-sharing effect is employed, the arm-level reliability can be represented by *k-out-of-n* system. An n-component system that works if and only if at least k components in the system are in a good state is called a *k-out-of-n* system (Way; Zuo, 2003). When k is less than n, the system has an inherent redundancy with $(m = n - k)$ spare parts. Therefore, the MMCC arm-level reliability can be evaluated through the sum of the probability of more than k cells inside a set of n are in good condition, given by (Tu; Yang; Wang, 2019):

$$R_{arm,kf}(x) = \sum_{i=k}^{n} C_n^i R_{cell}(x)^i (1 - R_{cell}(x))^{n-i}. \tag{4.1}$$

where C_n^i is the number of combinations in a group of i devices inserted into a set of n. In general, Eq. (4.1) as described by Eq. (3.22) when $n = k$.

As observed in Fig. 9, the three-phase DSCC-MMCC presents six arms in the structure. Assuming that each arm is independent and identical, the MMCC system-level reliability for active redundancy mode without load-sharing effect can be evaluated by:

$$R_{MMCC}(x) = \prod_{l=1}^{6} R_{arm,kf}(x). \tag{4.2}$$

4.3 Redundancy Factor Design

From the industry point of view, the converter shall be designed to achieve a reliability level $R(x_0)$ for a defined target lifetime x_0, regarding its specific application (Wang et al., 2014). Therefore, this work proposes a scheme to evaluate the redundancy factor which complies pre-defined reliability criterion. A combined reliability model that includes both constant and wear-out regions is employed.

The analytical calculation of the redundancy factor can be complex, since it requires the relationship of exponential terms, summation and combinations presented in Eq. (4.1). Therefore, the redundancy factor is numerically evaluated according to the flowchart of Fig. 40.

4.3.1 First Stage

First, the mission profile is defined for the considered application. Measurements of reactive power and ambient temperature mission profiles are employed in order to define the system operating condition. The most appropriate power devices can be selected according to the power rating, voltage and current levels.

4.3.2 Reliability Modeling

Initially, the cell-level reliability is calculated by Eq. (3.21). As observed, a combined reliability model proposed in chapter 3 that includes both constant and wear-out regions is employed.

The arm-level reliability can be evaluated through the *k-out-of-n* model, given by Eq. (4.1). Although in the first round of the algorithm the converter has only non-redundant k cells, the arm-level reliability presented in Eq. (4.1) is described by Eq. (3.22) when $n = k$.

Finally, the DSCC-MMCC system-level reliability can be evaluated by Eq (4.2) and analyzed for a given lifetime target.

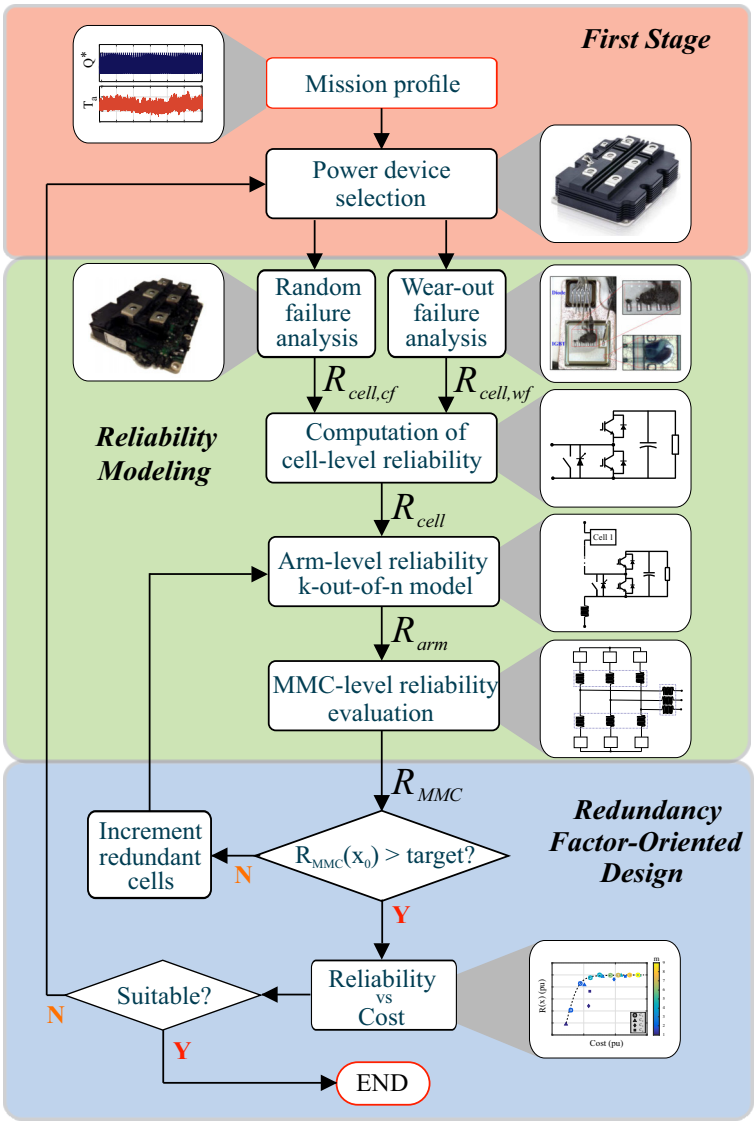

Figure 40 – Flowchart for the redundancy factor design.

4.3.2.1 Redundancy Factor-Oriented Design

The converter reliability requirement may be more stringent depending on the approach applied. For example, B_x approach is given according to the reliability-level such as:

- B_1 lifetime approach, the MMCC reliability $R_{MMCC}(x_0 = 20) \geq 0.99$.
- B_{10} lifetime approach, the MMCC reliability $R_{MMCC}(x_0 = 20) \geq 0.90$.

Since the required MMCC reliability is not met (e.g., $R_{MMCC}(x_0) < 0.99$), redundant cells shall be employed. Then, the number of redundant cells m is incremented until the reliability criterion is fulfilled (e.g., $R_{MMCC}(x_0) \geq 0.99$). Under such conditions, the

minimum required redundancy factor can be obtained as follows:

$$RF = \frac{m}{k}, \tag{4.3}$$

Regarding the overall cost of each design, the figure of merit employed includes the CAPEX and OPEX. The CAPEX is mainly related to investment in power electronics (e.g., semiconductor devices, controls, cabinets), which is dominant in the initial investment of the converter (Siddique et al., 2016). Thus, the cost of power electronics is based on the switching power installed as follows:

$$CAPEX = 12nK_cV_{svc}I_{svc}, \tag{4.4}$$

where V_{svc} is the device voltage class and I_{svc} is the rated device current. $K_c = 3.5$ €/kVA is employed (Siddique et al., 2016) in this work.

Moreover, the OPEX is mainly associated to the semiconductor conduction and switching losses (Tu; Yang; Wang, 2019). Therefore, the operational expenditure of the converter is considered as follows:

$$OPEX = K_oE_c(x_0), \tag{4.5}$$

where K_o is the price per kilowatt-hour and E_c is energy consumption of the converter. Based on loss penalty for transmission system, $K_o = 0.11$ €/kWh is employed (Alvarez et al., 2016). Thus, the overall cost is given by:

$$Cost = CAPEX + OPEX, \tag{4.6}$$

It is important to remark that the design which meets the MMCC reliability criterion at the lowest cost is the most suitable.

4.4 Results

In section 3 a reliability modeling of a DSCC-MMCC-based STACOM was presented. Although no reliability-level requirement has been applied to the results obtained, it can be stringent depending on the applied B_x lifetime approach. For example, all solutions presented reliability below the defined target for B_{10} lifetime approach. Under such conditions, the following analysis maintains the same case study presented in section 3.5. Aiming to improve the reliability of the DSCC-MMCC, active redundant cells are inserted into the converters structure.

The redundancy factor effect is analyzed in Fig. 41. As observed in Fig. 41 (a), when $m \geq 4$ for design C_{17}, the target is reached: $R_{MMCC}(20) \geq 0.99$. For $m \geq 6$, the increase in the number of redundant cells does not considerably affect the MMCC system-level reliability. The same principle is observed in other solutions. However, the target is reached for $m \geq 3$.

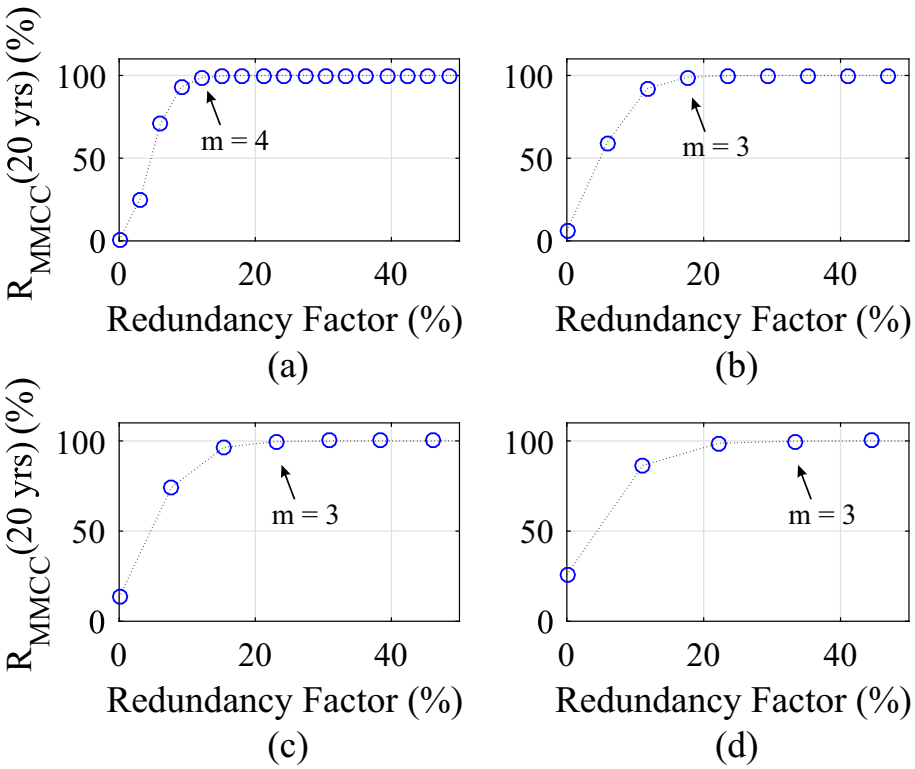

Figure 41 – MMCC system-level reliability at $x_0 = 20$ years with different redundancy factors: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

Figure 42 presents the variation of the MMCC system-level reliability as function of the redundancy factor. For design C_{17}, the MMCC reliability is $R_{MMCC}(20) = 0.67\%$ for $m = 0$, as observed in Fig. 42 (a). The system-level reliability is increased to 99.8% when a $RF = 15\%$ is applied, which corresponds to $m = 5$. Although the number of redundant cells is smaller $m = 3$ for design C_{65}, proportionally the redundancy factor used is higher $RF = 33\%$, as observed in Fig. 42 (d).

The overall cost of all solutions is shown in Fig. 43. Scenarios without redundant cells and with required RF for each case are analyzed. As observed, about 60% of the cost of the solutions is due to the CAPEX. Furthermore, CAPEX and OPEX are directly proportional to the number of cells. Thus, the overall converter cost increases as the redundancy factor increases. Indeed, the C_{65} solution is the most expensive design under such conditions.

Table 14 summarizes the results at $x_0 = 20$ years for all solutions proposed in this work. The converter energy consumption is evaluated according to the applied mission

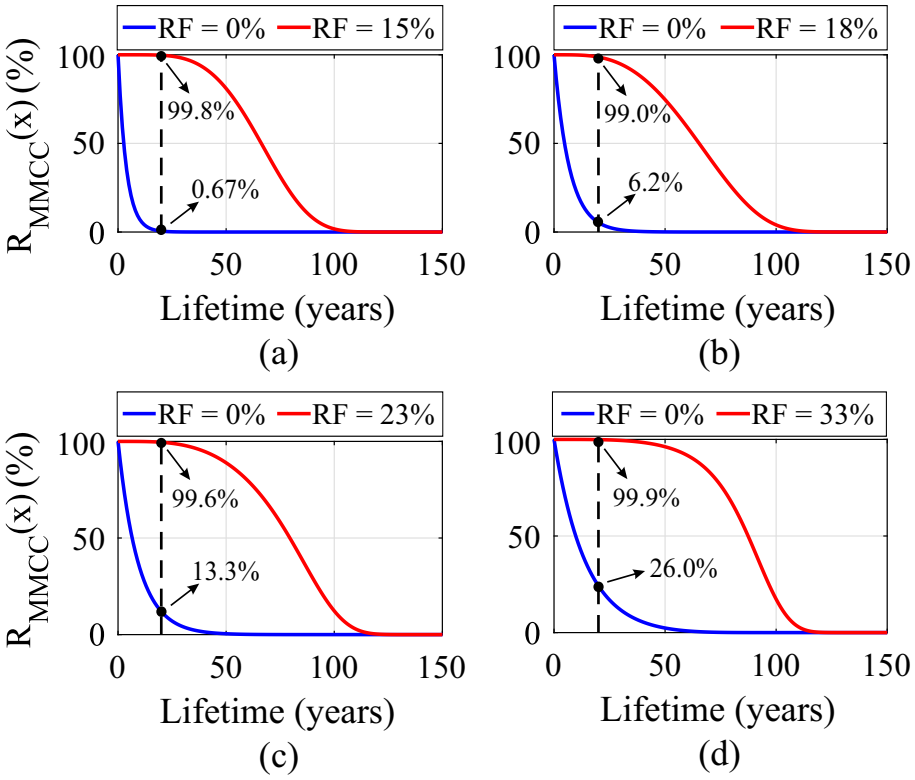

Figure 42 – MMCC system-level reliability function for 2 different redundancy factors: (a) C_{17}; (b) C_{33}; (c) C_{45}; (d) C_{65}.

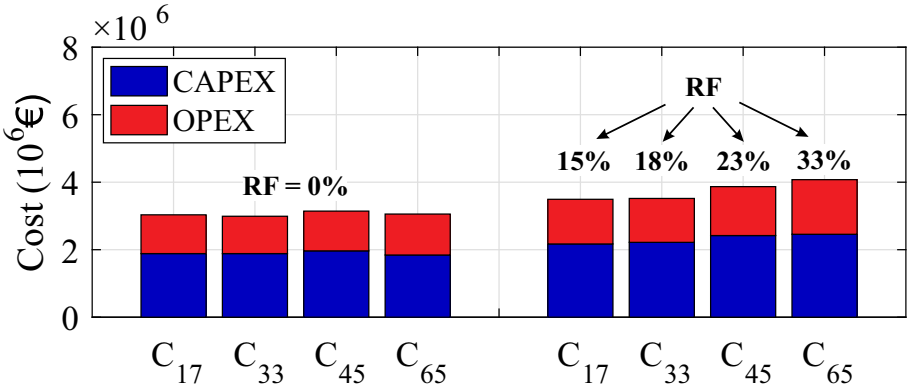

Figure 43 – Overall cost of all solutions divided into CAPEX and OPEX for 2 different redundancy factors.

profile of Fig. 29. As observed, when voltage rating of the power devices increases, the required redundancy factor increases. This is related to the number of converter cells (which reduces when the voltage increases) and with rounding (since the number of redundant cells must be integer). Although C_{33} presents the lowest energy consumption, the best cost-benefit for the B_1 approach refers to C_{17}.

Finally, Figure 44 presents the solutions cost for different reliability levels at $x_0 = 20$ years. As expected, the higher the system-level reliability required, the higher the cost of the solution. As can be seen, a line is traced for the best trade-off between cost and system-level reliability. The C_{17} solution with $m = 3$ ($RF = 9\%$) is the most suitable

Table 14 – Comparison of the redundant proposed designs for B_1 lifetime approach ($R_{MMCC}(20) = 99\%$).

Parameters	**C$_{17}$**	**C$_{33}$**	**C$_{45}$**	**C$_{65}$**
RF (%)	15.15	17.65	23.08	33.33
E$_c$ (GWh)	10.06	9.69	10.32	10.63
Cost (M€)	3.49	3.52	3.87	4.08

design for a reliability level greater than 90%. However, for more conservative designs, a reliability level $R_{MMCC}(20) = 99\%$ can be achieved with class C$_{17}$ and five redundant cells ($RF = 15\%$). In this case, the cost is increased by 5.6% due to the reliability improvement.

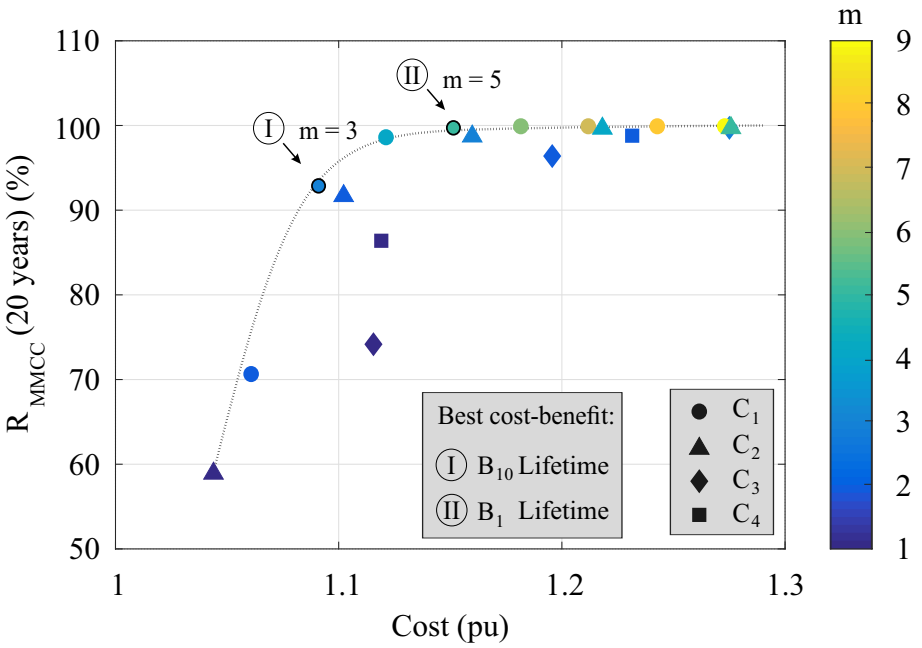

Figure 44 – *Reliability vs cost* of all MMCC solutions for different redundancy factors, considering a lifetime target of 20 years.

4.5 Chapter Conclusions

This work proposed a redundancy factor-oriented design methodology for DSCC-MMCC-based STATCOM. A scheme to evaluate the redundancy factor which complies pre-defined reliability criterion is proposed. A combined reliability model that includes both constant and wear-out regions is employed.

Four different realizations of the 17 MVA DSCC-MMC based STATCOM were compared in terms of cost and reliability level. As a result, 1.7 kV is the most cost-effective solution to achieve 99% of reliability level, during the whole target lifetime. It was concluded that the redundancy factor shall be chosen to achieve the required reliability with the minimum number of redundant cells.

The proposed methodology can be easily extended to other converter topologies and adapted to different cost evaluation methodologies. Finally, the most cost-effective solution for different reliability criteria can be evaluated.

5 Closure

This chapter recalls the conclusions and contributions of this Master thesis and is finished with directions for future work.

5.1 Conclusions

This work proposes a reliability-oriented redundancy design for DSCC-MMCC-based STATCOMs. The conclusions can be divided in two categories: Combined reliability modeling for DSCC-MMCC and redundancy factor design for DSCC-MMCC.

5.1.1 Combined reliability modeling for DSCC-MMCC

- When the rated blocking voltage of the HiPak power devices increases, the switching losses increase. Additionally, total diode conduction losses increase when the blocking voltage is higher, whereas this relationship is not straightforward for IGBTs.
- Regarding wear-out failure analysis, power modules baseplate solder is the most damaged region in this case study.
- The wear-out failures can be predicted (to some extent) and even avoided at the design stage. However, random failures play an important role in the converter lifetime analysis.
- Solutions based on power devices with higher blocking voltage presented higher reliability level considering both wear-out and random failure. Indeed, a converter with fewer components has higher reliability when random failure is dominant.

5.1.2 Redundancy factor design for DSCC-MMCC

- Redundant cells can be added to improve the converter reliability considering both wear-out and random failures.
- There is a minimum limit of redundant cells to achieve a reliability level $R(x_0)$ for a defined target lifetime x_0. Nevertheless, the increase in the number of redundant cells can cause dispensable costs.
- Overall converter cost increases for higher redundancy factors. Although the cost evaluation methodology can be changed, both CAPEX and OPEX increase when active redundancy without load-sharing is employed.

- The proposed reliability vs cost map allows the designer to choose the most cost-effective solution for a defined target. In the proposed case study, the targets set for 20 years of converter operation are 99% (B_1) and 90% (B_{10}) of reliability level. Under such conditions, a design based on 1.7 kV is the best solution.

5.2 Future Works

Some future topics derived from this Master thesis are presented as follows:

- Reliability methodology that combines both wear-out and random failures for other converter components such as capacitors, gate drivers, etc.
- A reliability model for both active and standby redundancy strategies. Additionally, evaluate the impact of each strategy on the lifetime and cost of the converter.
- Study the integration of battery energy storage systems in MMCC-based STATCOMs to provide both voltage and frequency regulation. In addition, evaluate the impact of system lifetime with battery banks.
- Employ reliability methodology for other applications such as HVDC systems and electrical drives. Compare other converter topologies as well as different power semiconductors devices technologies.

As observed, the possibilities of future work are many. The author really expects this research project can be continued in a possible Ph.D thesis.

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